New Devices and Architectures for Energy Efficient Computing

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The continuing evolution of silicon CMOS technology is clearly approaching some important physical limits. Since roughly 2003, the inability to reduce supply voltages according to constant-field scaling rules, combined with economic constraints on power density and total power, has forced designers to limit clock frequencies even as devices have continued to shrink. Either the device physics or the system architecture must change in a fundamental way if we are to escape this power-performance bottleneck. Recent years have brought a large increase in research funding and interest in new device concepts. Some of the devices explored to date, such as tunneling field-effect transistors (TFETs) promise to open a new low-power design space which is inaccessible to conventional FETs. Nanomagnetic devices may allow memory and logic functions to be combined in novel ways. And newer, perhaps more promising device concepts continue to emerge. At the same time, research in new architectures has also grown. Indeed, at the leading edge, researchers are beginning to focus on co-optimization of new devices *and* new architectures. While neuromorphic devices and architectures are generating much of the current excitement, a vast landscape of additional research opportunities is yet to be explored.