Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

nanoelectronics RESEARCH INITIATIVE

Update on the Nanoelectronics Research Initiative

NSF Grantees Meeting
December, 2009

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Director
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Semiconductor Research Corporation

A Family of Distinct, Related Program Entities

GRC

Global Research Collaboration

Ensuring vitality of current industry

FCRP

Focus Center Research Program

Breaking down barriers to extend CMOS to its limits

NRI

Nanoelectronics Research Initiative

Beyond CMOS – identify next information element

Education Alliance for Science, Engineering & Technology

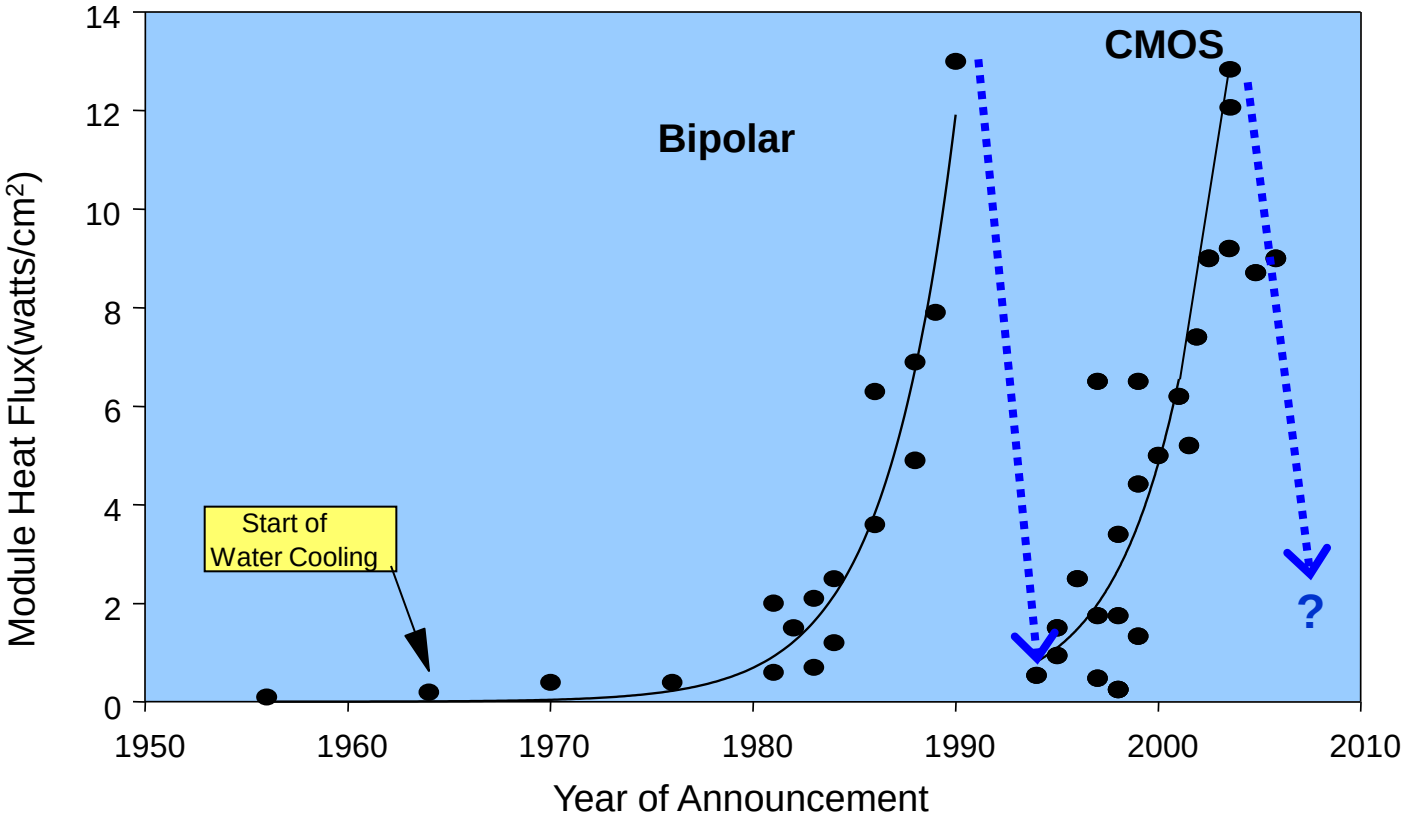
Attracting and educating the next generation of innovators and technology leaders

TRC's

Topical Research Collaborations

Topic(s) chosen by participants

CMOS Scaling: Power is ***THE*** Issue



- 2005 ~ 2015: New technology enhancements → FCRP Goal
  - Continued CMOS shrinking, low-power devices, multi-core chips, 3D packaging, new memory devices, etc.
- > 2015? : New device? → NRI Goal

Beyond CMOS Logic: What to look for?

- To beat the power problem requires:
  - A device with a lower energy, room temperature switching mechanism

    or
  - A system that operates out of equilibrium or recovers operation energy as part of the logic computation

- **Required characteristics:**
  - **Scalability**
  - **Performance**
  - **Energy efficiency**
  - **Gain**
  - **Operational reliability**
  - **Room temp. operation**

- **Preferred approach:**
  - **CMOS process compatibility**
  - **CMOS architectural compatibility**

Alternative state variables

- Spin–electron, nuclear, photon
- Phase
- Quantum state
- Magnetic flux quanta
- Mechanical deformation
- Dipole orientation
- Molecular state

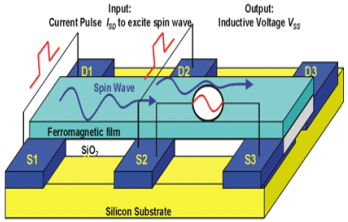
NRI Mission Statement

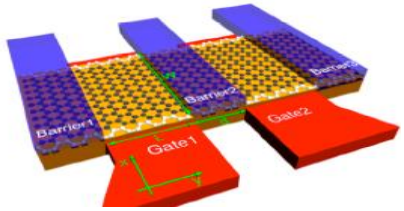
NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

- These devices should **show significant advantage over ultimate FETs** in power, performance, density, and/or cost to enable the semiconductor industry to **extend the historical cost and performance trends** for information technology.
- To meet these goals, NRI pursues **five research vectors**, focused on discovering and demonstrating new devices and circuit elements for doing computation.
- Finally, it is desirable that these technologies be **capable of integrating with CMOS**, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

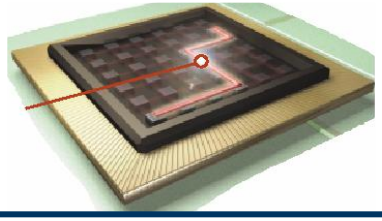
NRI Primary Research Vectors

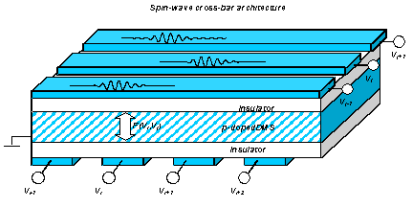
- **NEW DEVICE**
  Device with alternative state vector



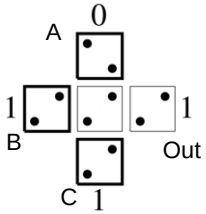


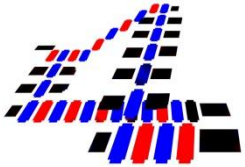
- **NEW WAYS TO CONNECT DEVICES**
  Non-charge data transfer



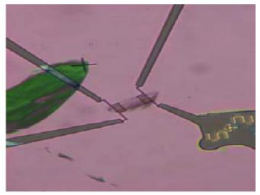


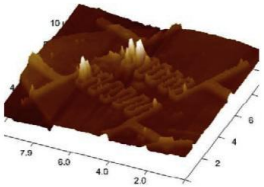
- **NEW METHODS FOR COMPUTATION**
  Non-equilibrium systems



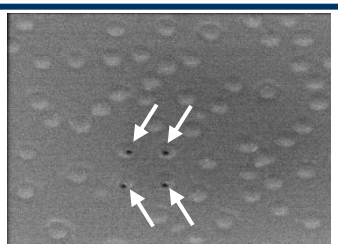


- **NEW METHODS TO MANAGE HEAT**
  Nanoscale phonon engineering





- **NEW METHODS OF FABRICATION**
  Directed self-assembly devices



NRI Funded Universities

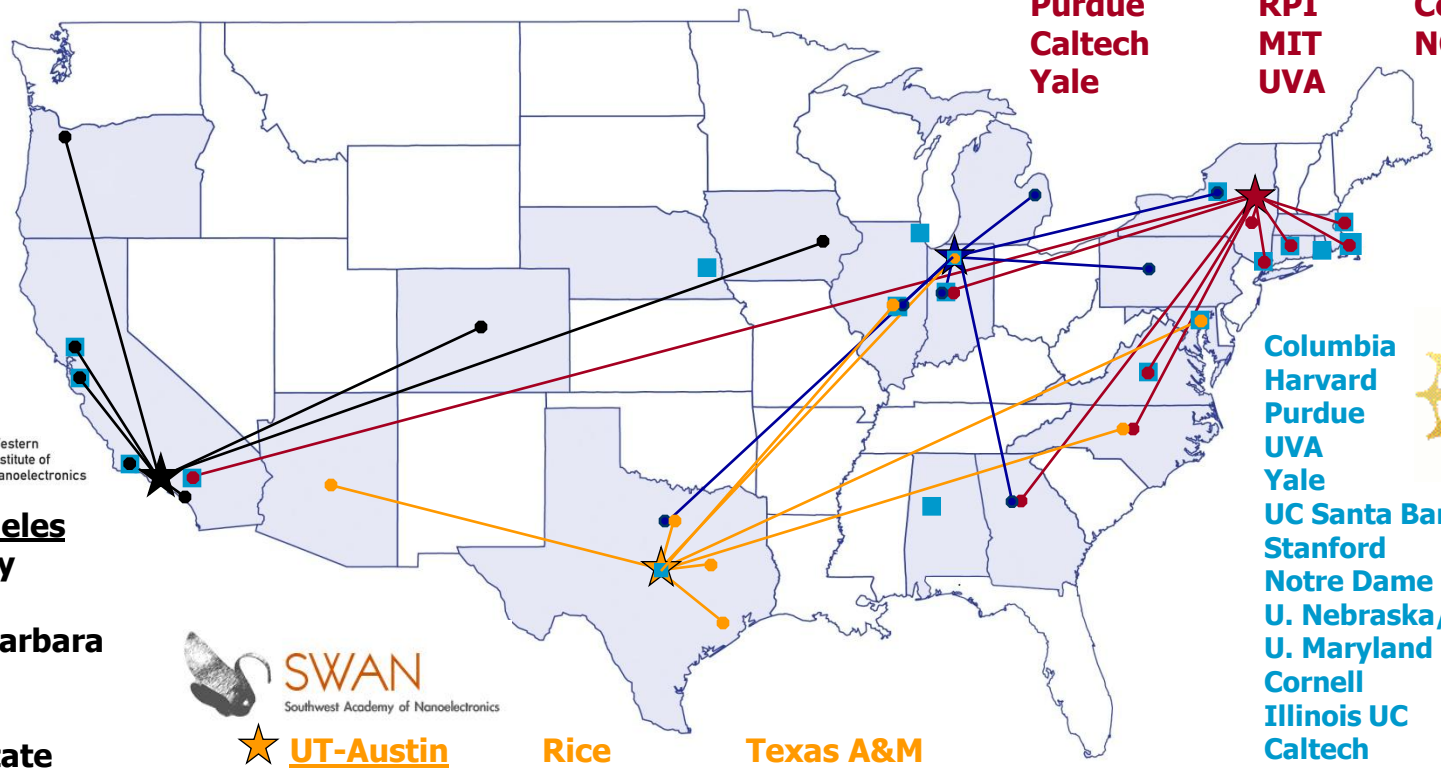
Finding the Next Switch

Nanoelectronics • Architectures MIND MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

★ **Notre Dame**
Illinois-UC
Michigan
Cornell
Purdue
Penn State
UT-Dallas
GIT

INDEX INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

★ **SUNY-Albany**
Purdue
Caltech
Yale
GIT
RPI
MIT
UVA
Harvard
Columbia
NCSU



W/N Western Institute of Nanoelectronics

★ **UC Los Angeles**
UC Berkeley
UC Irvine
UC Santa Barbara
Stanford
U Denver
Portland State
U Iowa

SWAN Southwest Academy of Nanoelectronics

★ **UT-Austin**
UT-Dallas
U. Maryland
Rice
ASU
NCSU
Texas A&M
Notre Dame
Illinois UC

NSF

Columbia
Harvard
Purdue
UVA
Yale
UC Santa Barbara
Stanford
Notre Dame
U. Nebraska/Lincoln
U. Maryland
Cornell
Illinois UC
Caltech
UC Berkeley
MIT
Northwestern
Brown
U Alabama

Over 30 Universities in 20 States

NRI: A *Goal-oriented*, *Basic* Research Program

- Integrating work across the 4 NRI-NIST centers and the 18 projects at 15 NSF Nanoscience Centers

WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Iowa, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas, Cornell, GIT
Spin devices Spin circuits Benchmarks & metrics Spin Metrology	Novel state-variable devices Fabrication & Self-assembly Modeling & Architecture Theory & Simulation Roadmap Metrology	Logic devices with new state-variables Materials & structures Nanoscale thermal management Interconnect & Arch Nanoscale characterization	Graphene devices: Thermal, Tunnel, & Spin Interband Tunnel Devices Non-equilibrium Systems Model / Measurement Nanoarchitecture

NSF-NRI Projects

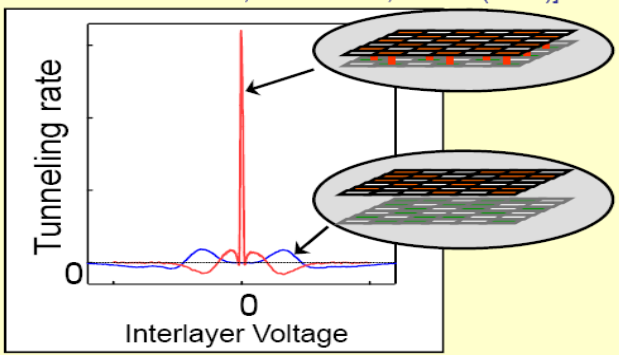
Co-funding 18 Projects at 15 NSF Centers

Caltech MRSEC	*2008: Graphene Atomic Switches for Ultracompact Logic Devices and NV Memory*
Columbia NSEC	*2008: New Graphene-Based Switching Devices: Electron Wavefunction Focusing and Pseudo-Spin Switching*
Cornell NSEC	*2007: Controlled Orbital Hybridization in the CNT Quantum-Modulated Transistor*
Harvard NSEC	*2008: Tunable Ultra-fast Conductance Switching through External Fields*
Purdue NCN	*2007: Exploratory Theory, Modeling, and Simulation for the NRI* *2008: Experimental Realization of Low-power Transistors with Negative Capacitors* *2009: Exploration of Novel All-Spin Logic (ASPL) for Device-Circuit-Architecture*
Stanford NSEC (UI-UC)	*2008: Ultra-Low Power Pseudospintronic Switching in Bilayer Graphene at Rm T*
U. Maryland MRSEC	*2007: Pseudospintronics (UT-Austin)* *2008: Controlling the Electronic Properties of Graphene*
U. Nebraska MRSEC	*2007: Multiferroic Interfaces: New Paradigms for Functional Switching*
UVA MRSEC (Notre Dame, UCSB)	*2007: Coherent Spin Dynamics in Single Ion-doped Semiconductors: Towards a Coherent or Quantum Spin Switch*
Yale MRSEC	*2007: Design and Fab of Magnetic-based Devices with Complex Oxide Materials*
UC-Berkeley NSEC	*2009: Spin-Oscillators for Non-Charge Based Ultra Low Power Logic and Comm.*
MIT MRSEC (UVA)	*2009: Reconfigurable Array Magnetic Automata (RAMA)*
Northwestern MRSEC	*2009: Generating, Probing, and Manipulating Excitons in Carbon Nanomaterials*
Brown MRSEC	*2009: Direct-Write Synthesis of Graphene Devices*
Univ. of Alabama MRSEC	*2009: Spintronic Logic Devices*

Bilayer pseudoSpin FET

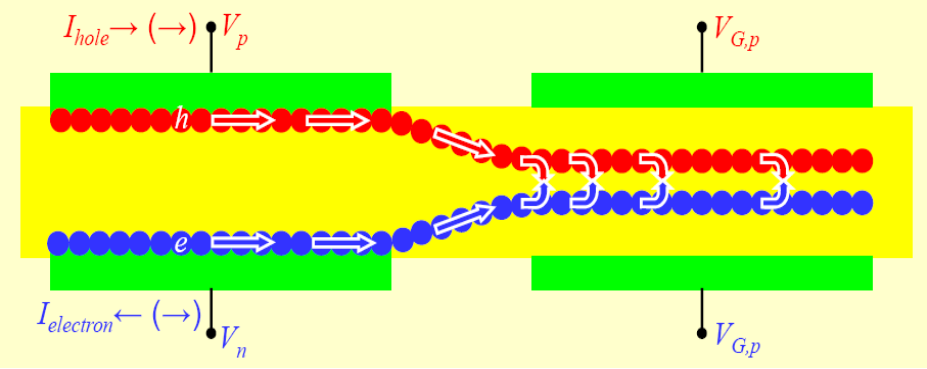
Banerjee, Register, MacDonald, et al., UT-Austin

[Eisenstein Lab Cal Tech, JPE & AHM, Nature (2004)]

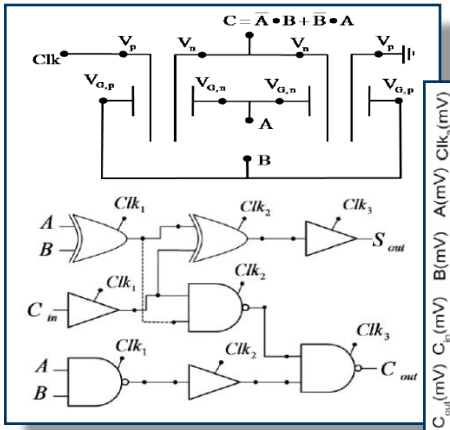


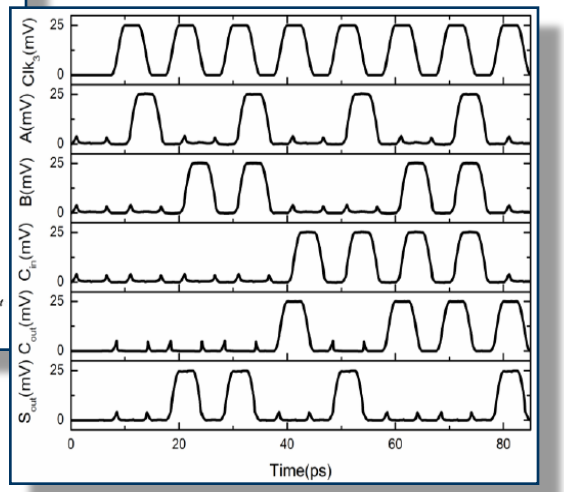
Low temp., condensation-based electron-hole tunneling in bilayers between half-filled Landau levels

Room temp. condensation in ***graphene*** – a "perfect storm" of material properties: • electron-hole symmetry • low DOS • gapless • mono-atomically thin layers



BiSFET with ***gate-control*** over the condensate [1]





SPICE simulations (1-bit adder) (with Carpenter)

Simulated devices and basic logic gates in SPICE

- Inverter with complementary BiSFET design simulated at
  f_{CLK} = 100 GHz
  V_{DD} = 25 mV
  $E_{inverter}$ = 0.008 aJ → just 2x the Landauer limit

[1] Banerjee, Register, Tutuc, Reddy & MacDonald, IEEE EDL **30**, 158 (2009); [2] Basu, Register, MacDonald & Banerjee, TechCon 2009.; [3] Reddy, Register, Tutuc & Banerjee, IEEE TED, in review;

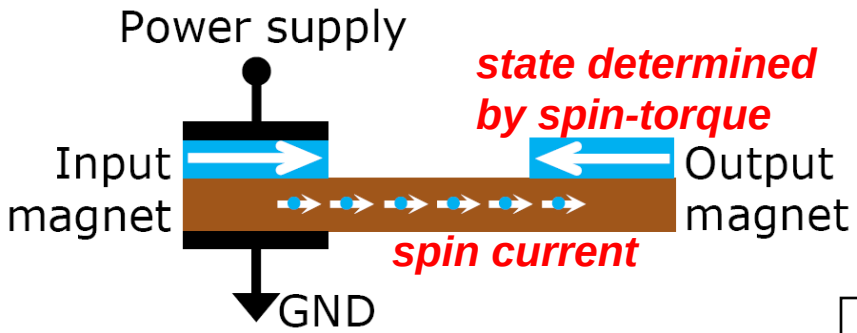
All-Spin Logic

Salahuddin, Datta, et al., Purdue

❑ Proposed all-spin logic:

Information: *state of magnet*

Communication: *spin currents*



Magnets are natural digital spin capacitors

❑ CMOS logic:

Information: *charge on capacitor*

Communication: *charge currents*

B. Behin-Aein, D. Datta, S. Salahuddin & S. Datta, to appear in *Nature Nanotech.*

❑ Rationale: Dramatic reduction in E_S

NΔE for CMOS → ΔE for all-spin

N = # of electrons or spins

ΔE = energy barrier for noise immunity

➢ Generic result for all switches based on collective states ("magnets")

❑ Features:

- Room temperature operation
- Physics and technology already demonstrated
- No magnetic fields

Estimated performance parameters (ΔE~40kT)

❖ **Inverter (FO4)**	Energy	Area	Delay
ASL	ΔE ~ 0.0002 fJ	0.008um^2	3 ps
CMOS^{15nm}	N ΔE ~ 0.08 fJ	0.03 um^2	4 ps

❖ **32 bit adder**	Energy	Area	Delay
ASL	ΔE ~0.4 fJ	0.5 um^2	500 ps
CMOS^{15nm}	N ΔE ~13 fJ	24um^2	200 ps

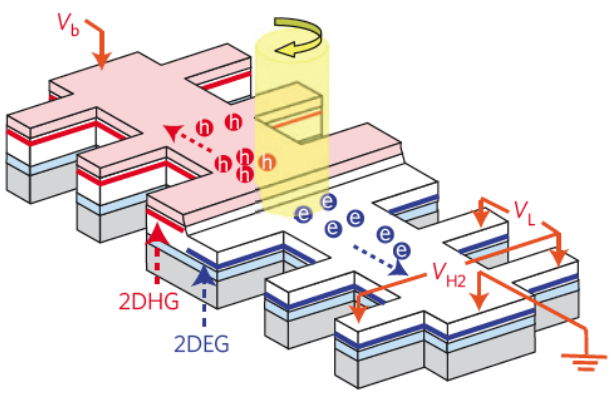
RT SpinFET Proof-of-Concept

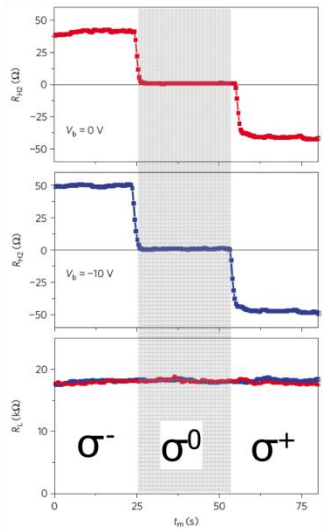
Sinova, TAMU

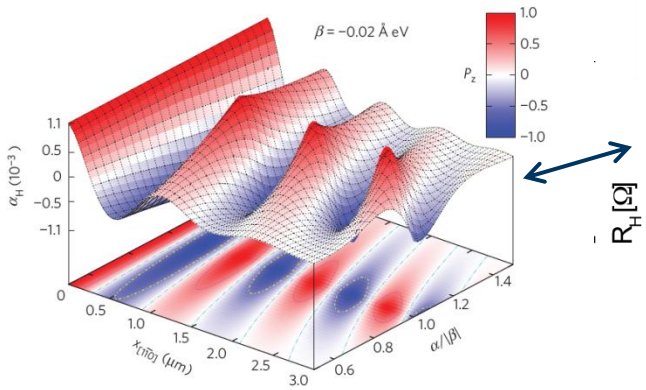
nature physics
ARTICLES
PUBLISHED ONLINE: 2 AUGUST 2009 | DOI: 10.1038/NPHYS1359

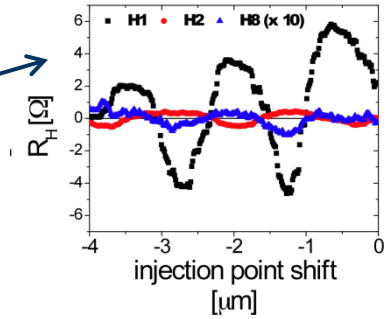
Spin-injection Hall effect in a planar photovoltaic cell

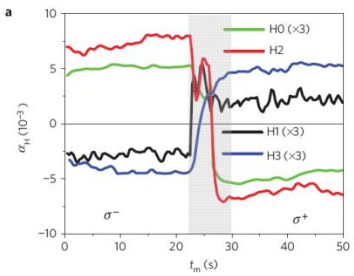
J. Wunderlich[1,2]*, A. C. Irvine[3], Jairo Sinova[2,4], B. G. Park[1], L. P. Zârbo[4], X. L. Xu[1], B. Kaestner[5], V. Novák[2] and T. Jungwirth[2,6]

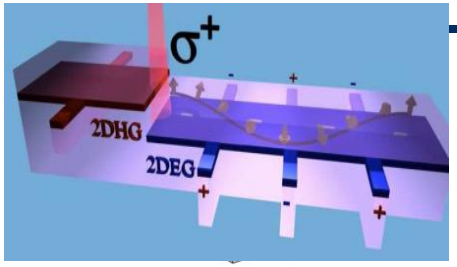


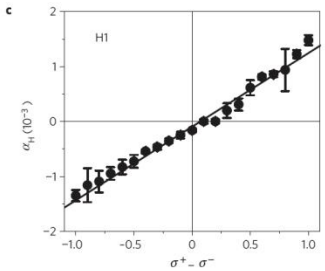


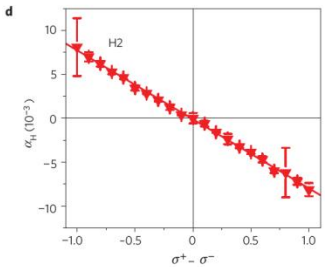










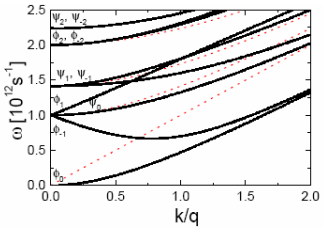


- **electrical** detection method for Spin current
- **large signal** (comparable to AHE in metallic ferromagnets)
- **high spatial resolution** (~ < 50nm)
- **nondestructive** detection of spin WITHOUT magnetic elements
- **linear** with degree of spin polarization
- **high temperature** operation
- first electrical detection of the **Spin Helix** (coherently precessing spins)
- **all electrical polarimeter** (transfers degree of light polarization into an electrical signal)

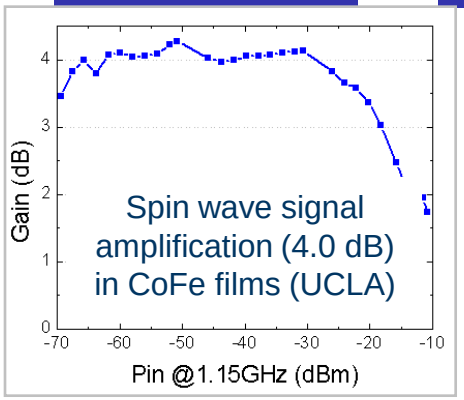
Project Pathway: Spin Waves

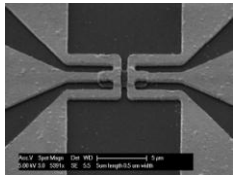
Western Institute of Nanoelectronics

2007 | **2008** | **2009** | **next**

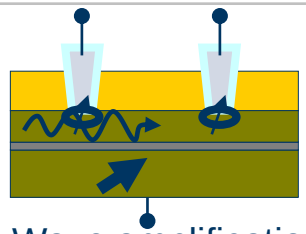


Simulation of spin wave generation by electric field (UCB)

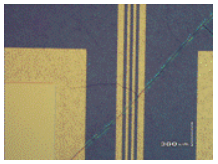




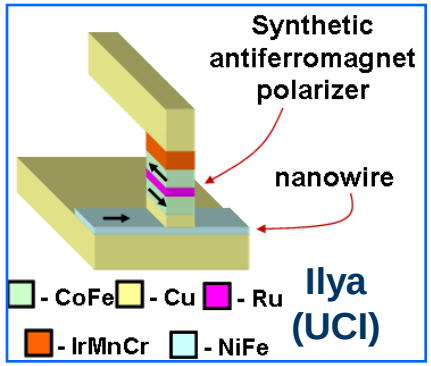
Spin waveguides (UCSB)



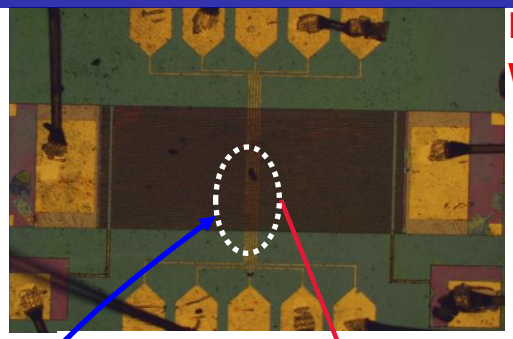
Spin Wave amplification via spin torque concept (Stanford, UCSB, Intel)



Fabricated structures using PZT and BFO (UCLA/UCB)

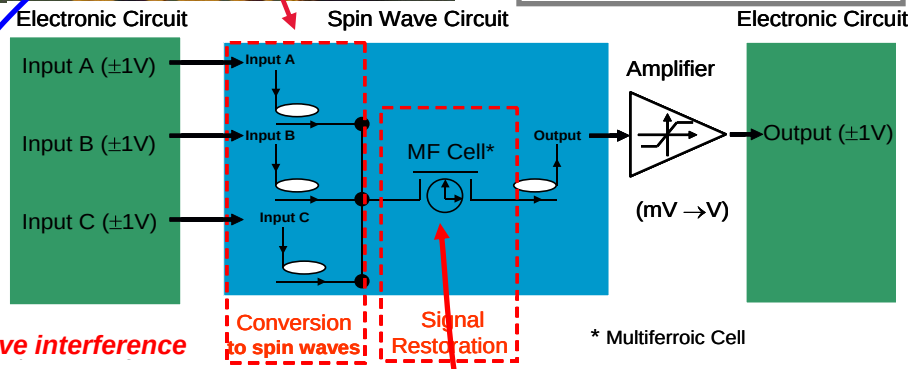


Ilya (UCI)

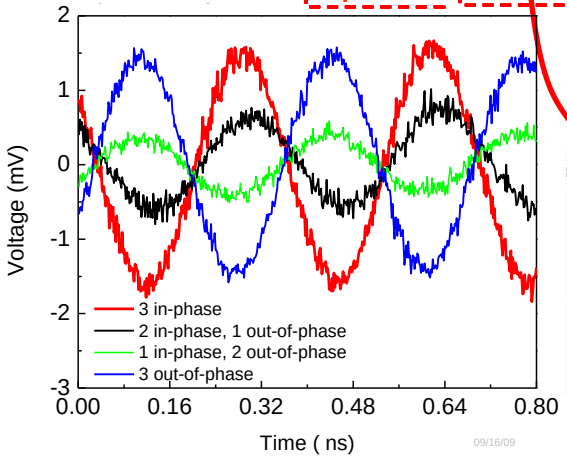


Five-terminal spin wave device (UCLA)

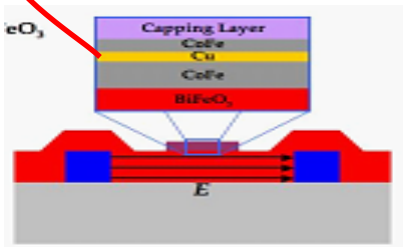
Integration of the spin wave elements



Spin wave interference

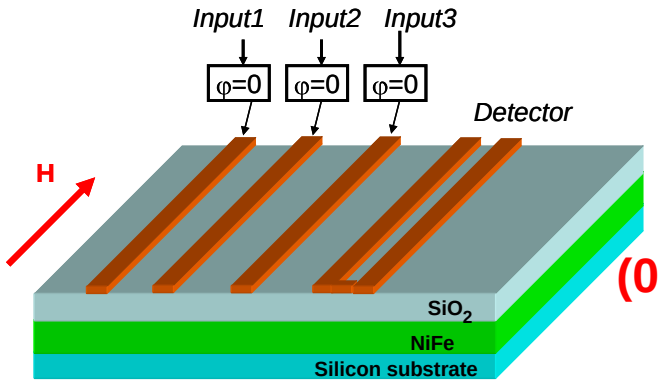


Electric Field control of spin waves (UCB)

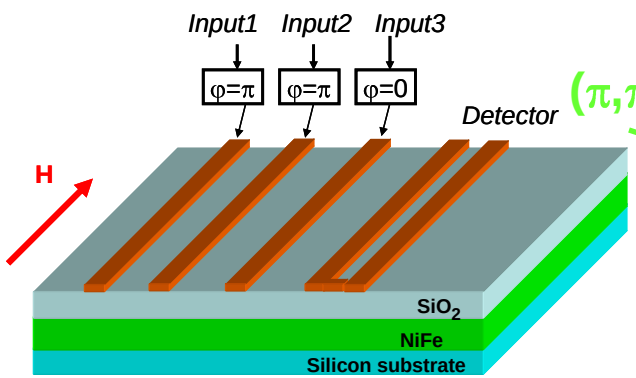


Spin Wave Majority Gate

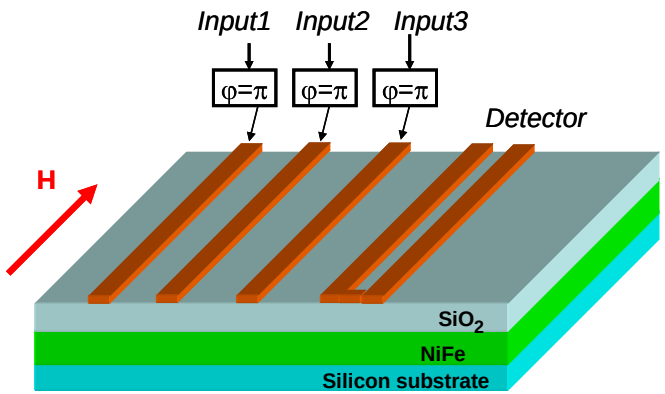
Khitun, UCLA



(0,0,0) → 0



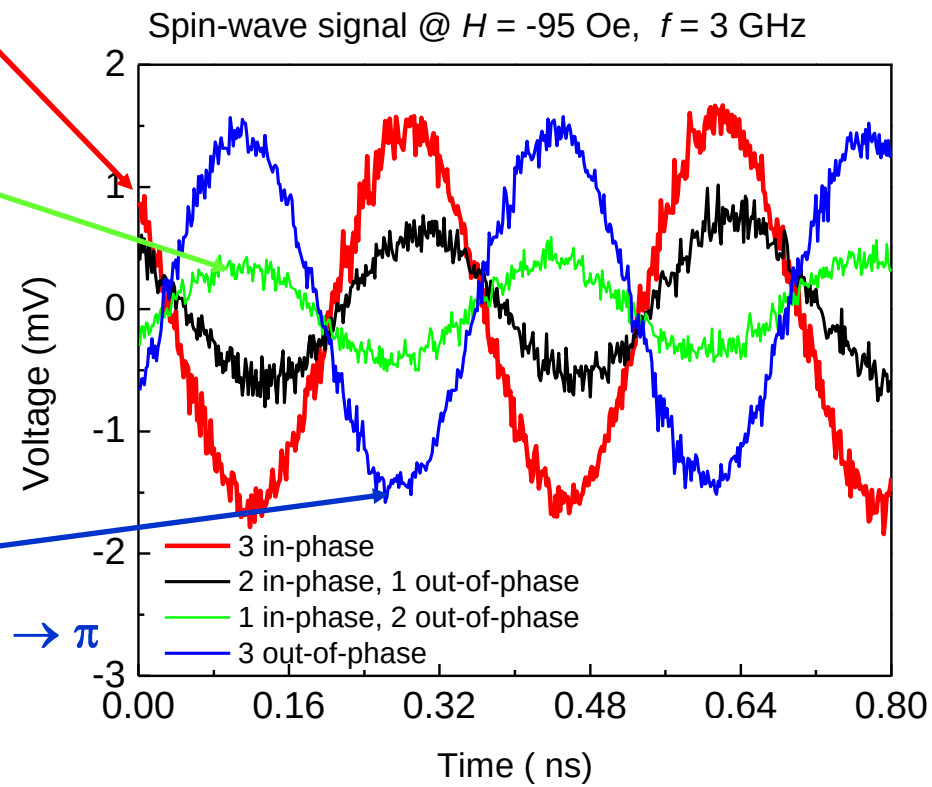
(π,π,0) → π



(π,π,π) → π

Achievement 2009

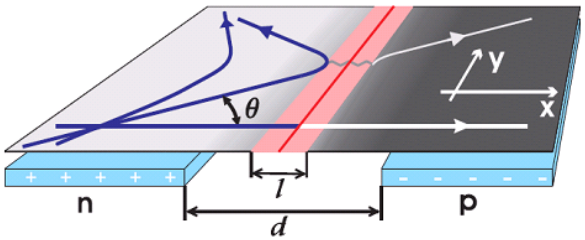
- **Demonstration of a five-terminal spin wave device**
- **Potential for running multiple signals at different frequencies**



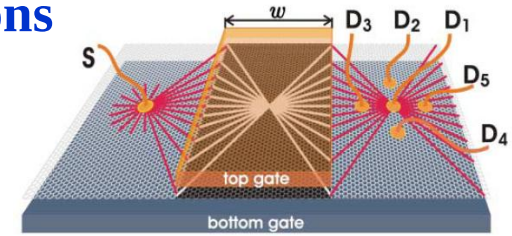
Veselago Lens Devices

Lee, Geer, et al., SUNY-Albany

INDEX Thrust: Graphene PN Junction Devices for Optics-like Manipulation of Electrons



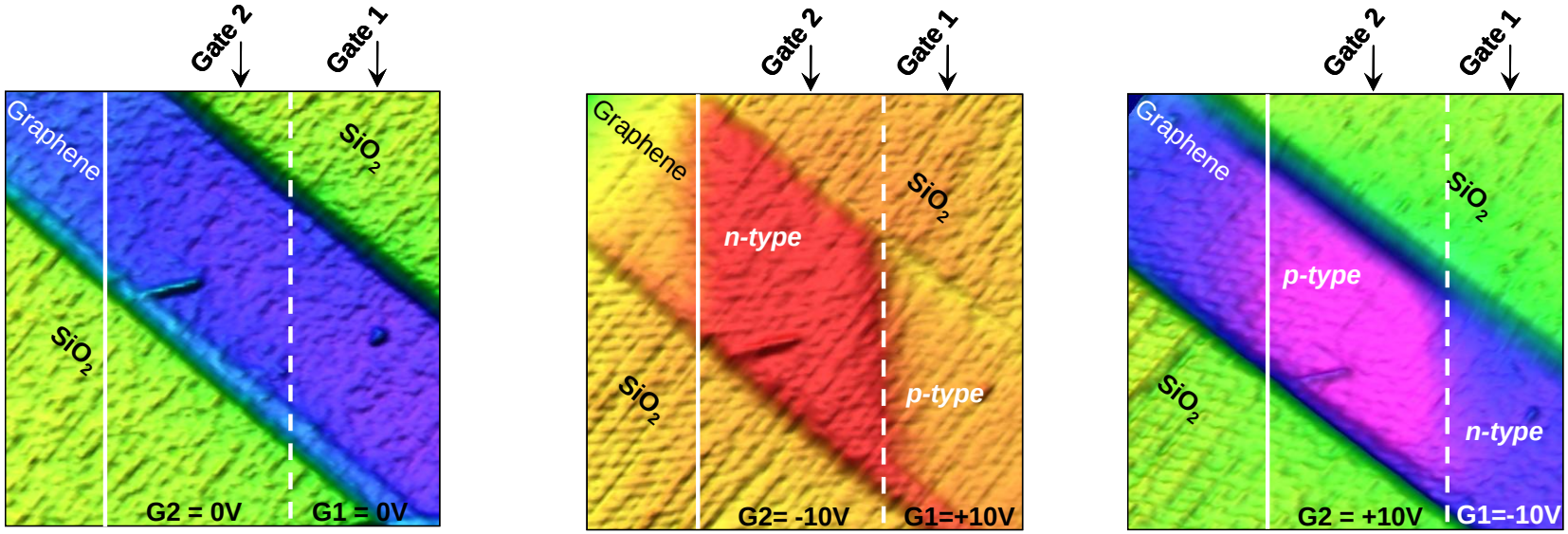
V.V. Cheianov and V.I. Fal'ko, PRB 74, 041403 (2006).



Science 315 (2007)

- **Total Internal Reflection**
- **Electron Focusing (Veselago Devices)**

Kelvin Probe Microscopy to probe Graphene PN Junction Bulit-in Potential



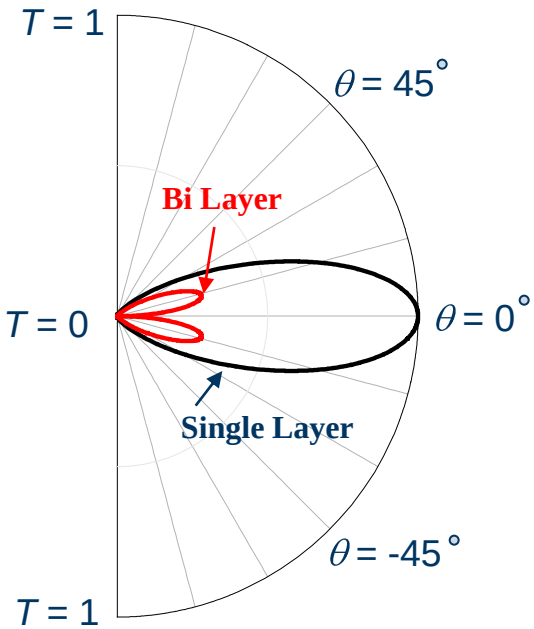
Left image: **No voltage** Center image: **+ 20V differential** Right image: **- 20V differential**

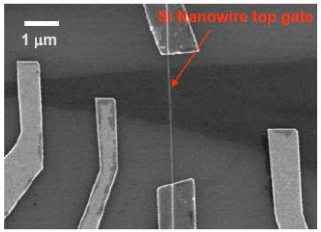
▪DEMONSTRATION OF DIRECT IMAGING OF DOPING GRADIENT

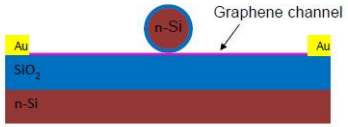
Bilayer Heterojunction Devices: Beam Splitter

Kim, Columbia

Transmission Probability

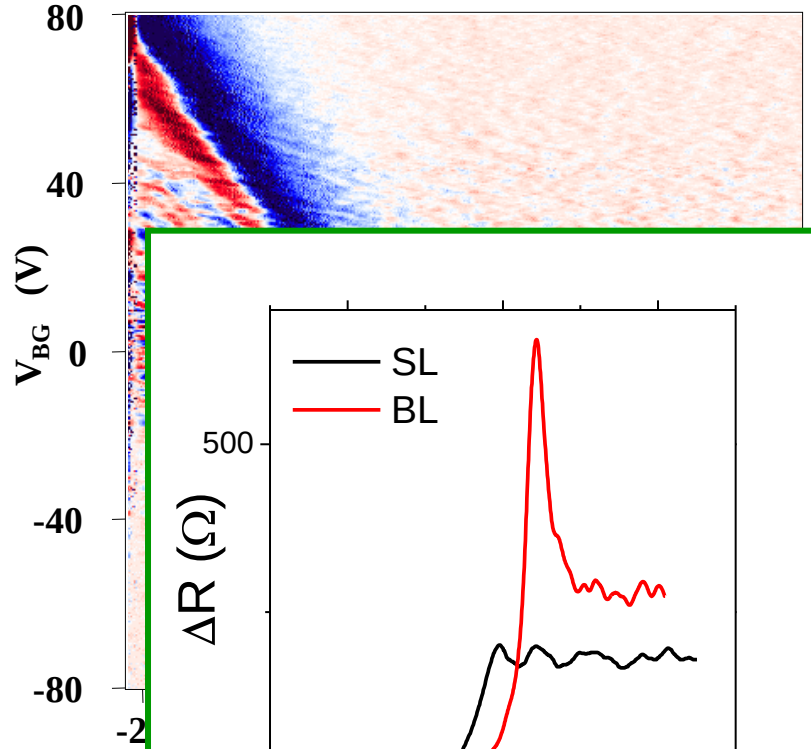






Si Nanowire: diameter ~ 25 nm
Natural SiO_2 dielectric ~ 2 nm

Transport in Graphene bilayer heterojunctions



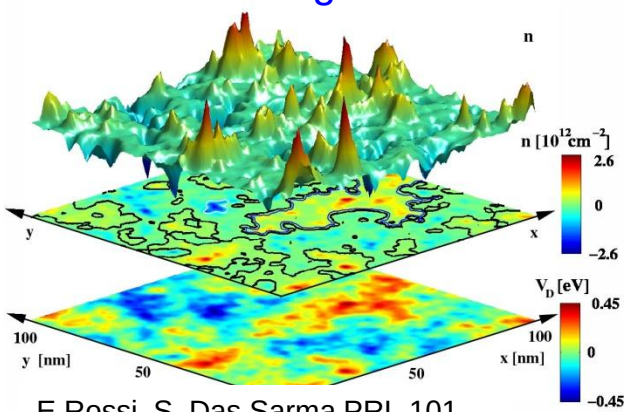
Single Layer:
No back scattering
- Klein Tunneling Beam Collimator

Bi-Layer:
No forward scattering
- Anti Klein Tunneling Beam Splitter

Transport in Dis-ordered Graphene

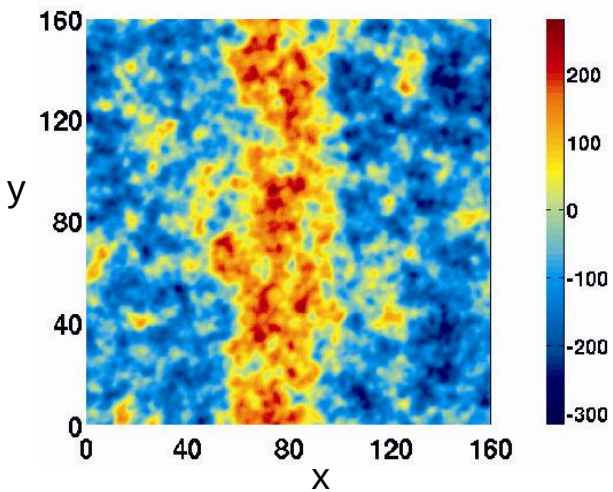
DasSarma, Hwang, Rossi, UMD

Characterized disorder-induced inhomogeneities



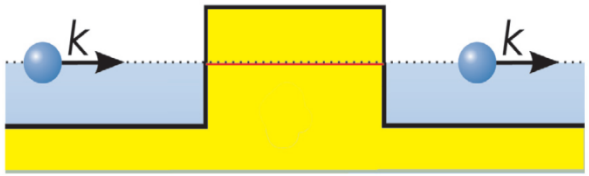
E.Rossi, S. Das Sarma PRL 101, 166803 (2008); APS invited talk.

Screened disordered potential in p-n-p graphene junction



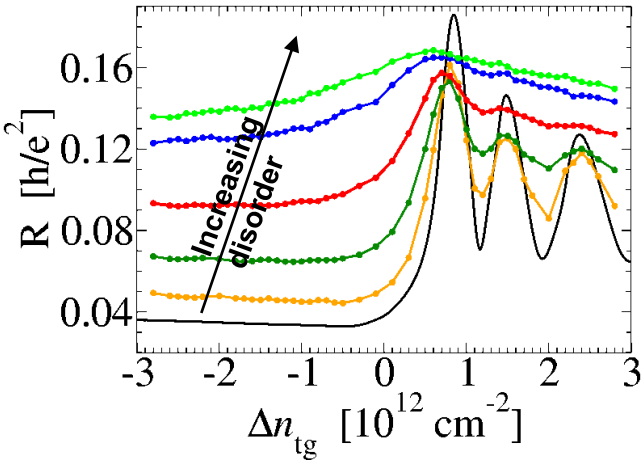
Klein tunneling in disordered graphene p-n-p junctions

Developed quantum transport model with microscopic treatment of charge disorder.



E. Rossi, J.H. Bardarson, P.W. Brouwer, S. Das Sarma, arXiv:0908.3674

Evolution of resistance oscillations characterizing the Klein tunneling, with increasing disorder.



NRI Device & Architecture Benchmarking

Led by Kerry Bernstein & MIND Center

- Approach
  - Survey NRI emerging device technologies on quantitative and qualitative benchmarks
  - Evaluate performance for a given computational function (such as an adder or PLA element) compared to CMOS 15nm projections
  - Consider alternate architectures that match unique device behavior for specific application areas / accelerators

- By the numbers:
  - 83 Researchers at all NRI Centers from 14 Universities, 7 corporations, and 3 government agencies actively participated
  - 461 files were submitted, containing 665MB of data
  - Initial readout at MIND Review and a joint NRI-NSF Workshop, August 2009
    - "Architectures for Post-CMOS Switches" Notre Dame (NSF: P. Mazumder)

- Using results to identify most promising device areas and to identify key questions / challenges to be focused on for specific devices
  - Keeping in sync with ITRS Emerging Research Devices and Architectures Working Groups
  - IEEE Proceedings paper planned for 2010

NRI Benchmarking
Initial Devices

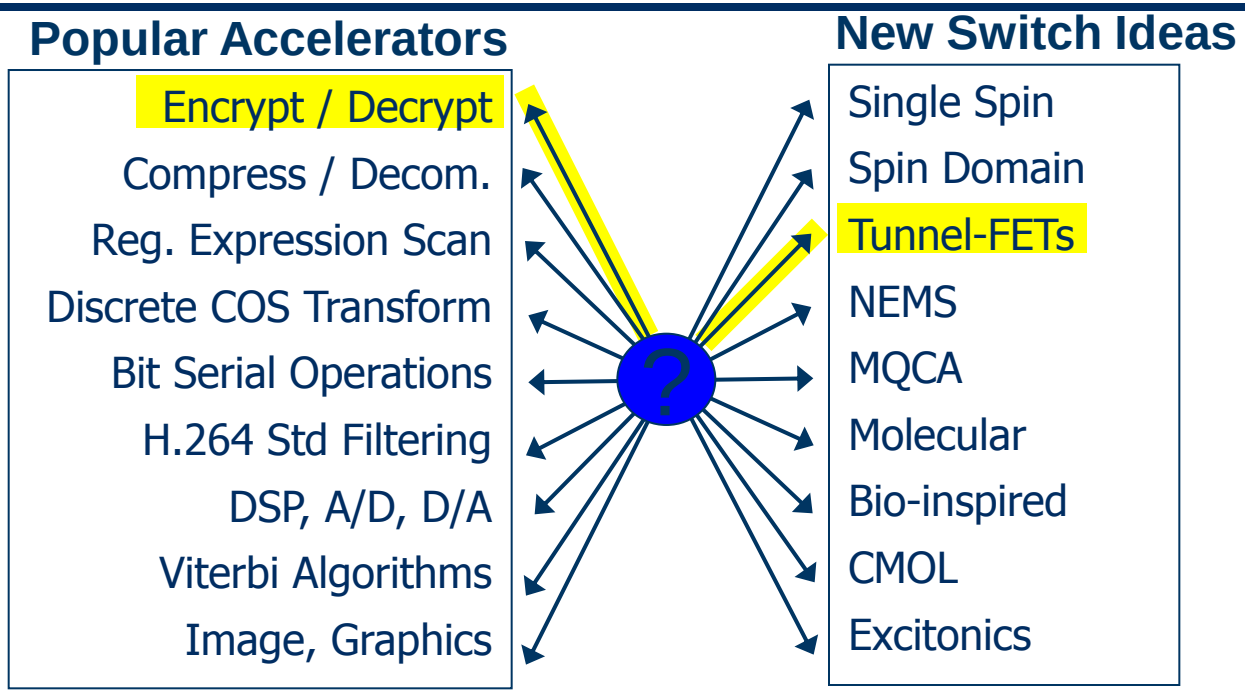
Switch	PI	Institution	Center
Mag Tunnel Jct	Markovic	UCLA	WIN
Spin Wave Devices	Khitun	UCLA	WIN
Multiferroic	Salahuddin	UCB	WIN
Few Spin	Flatte	Iowa	WIN
BiSFET	Register	UTA	SWAN
RIEFET	Register	UTA	SWAN
HetTFET	Register	UTA	SWAN
Veselago Devices	Lee	SUNY	INDEX
Excitons	Baldo	MIT	INDEX
Mag Rings	Ross	MIT	INDEX
All-Spin Logic	Behin-Aein	Purdue	INDEX
Tunnel FETs	Seabaugh	Notre Dame	MIND
Nanomag / MQCA	Niemier	Notre Dame	MIND
Graphene Thermal	Chen	Purdue	MIND
SET/BDD	Datta	PSU	MIND
Graphene SpinFET	Ye	Purdue	MIND

NRI Benchmarking
Alternate State Variables Covered

Information Tokens	Transport Mechanisms
Spin waves	Drift
Spin (Single and Few)	Diffusion
Magnetic Field (Collective Spin)	Ballistic Transport
PseudoSpin	Spin Conduction
Heat	Electromagnetic Waves
Excitons	Simple Conduction Band Transport
Plasmons	EM quasi-particle in surface plasmon-polariton mode
Charge	

- Focusing on potential advantages / challenges of broad range of alternate state variables
  - Primary advantages: Power, Area
  - Primary challenges: Speed
- Explicit focus on the impact of communication between devices to build logic gates
- Current work focused on CMOS-based architectures – favors charge-based devices
  - Need increased focus on architectures matched to specific devices
  - Consider parallel architectures, multi-bit or multi-level logic, application-specific architectures to mitigate lower speed operation

Matching Functions & New Switch Behaviors



Example: Cryptography Hardware Acceleration

Operations required:	Rotate, Byte Align, XORs, Multiply, Table Lookup
Current CMOS circuits:	Transmission Gates (“T-Gates”)
New Switch Opportunity: (example)	A number of new switches (i.e. T-FETs) don’t have thermionic barriers: won’t suffer from CMOS Pass-gate V_T drop, Body Effect, or Source-Follower delay.
Potential Opportunity:	Replace **4** T-Gate MOSFETs with **1** low power switch.

Take-aways

- Power will continue as the principal scaling issue for CMOS
  - CMOS will continue to scale over at least the next decade, with emphasis on utilizing increasing transistor density over increasing frequency
- Any new technology must overcome the power / performance limits of a charge-based FET to continue the scaling trend of increased function / dollar
  - Does the device offer potential for lower energy storage / operation than CMOS?
  - Does the computation system offer potential for non-equilibrium or energy-recovery in operation?
- The NRI centers and NRI-NSF projects are working together to focus on key questions for specific devices
  - Demonstrating more phenomena at room temperature
  - Finding ways to increase the magnitude of novel effects
  - Performing experiments to verify key predictions from theory and simulation
- Need to expand the focus beyond the single device, to consider appropriate architectures (potentially application-specific) for doing computation
  - Engage with industry and university circuit / architecture contacts to look at architectures (circuits, logic gates, memory, etc.) to match device function
  - Expand benchmarks to facilitate higher level comparisons: "logical effort", computational through-put, and performance on key algorithms ("7 Dwarves")

Questions? More Information?
http://nri.src.org

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Other Resources: http://www.itrs.net → 2009 Editions coming soon
Emerging Research Devices & Materials Reports