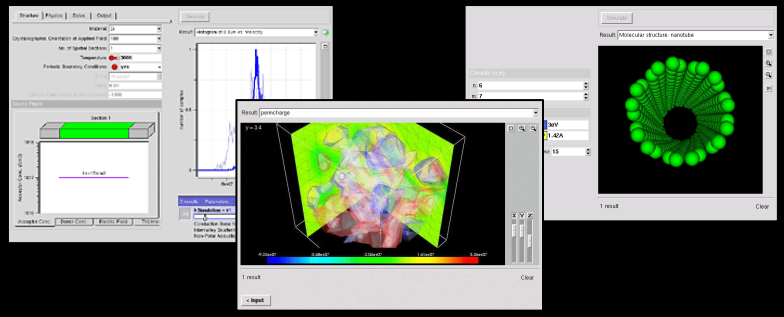
nanoHUB.org
Future Cyberinfrastructure serving over 26,000 users today

Gerhard Klimeck,
Mark Lundstrom, Michael McLennan, George Adams
Network for Computational Nanotechnology
Purdue University

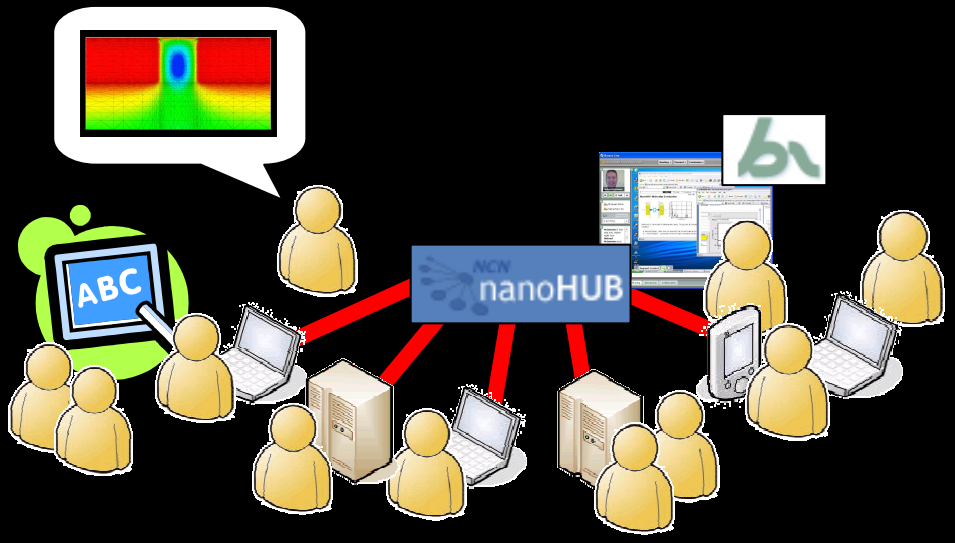
NSF Grantee's Meeting
December 4th, 2007

What is nanoHUB?

Online simulation…



…and more!



[Live Demo>>]

[PPT Demo>>]

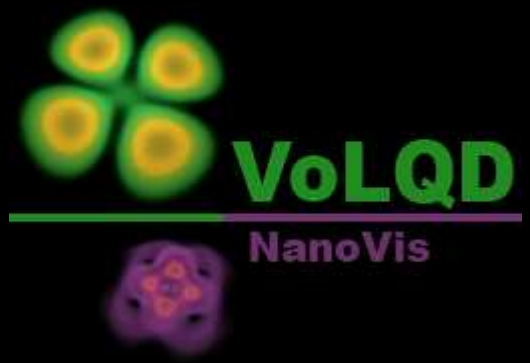
[Long PPT Demo>>]

Free Account

(just confirm your email address)

Interactive Visualization

integrated seamlessly

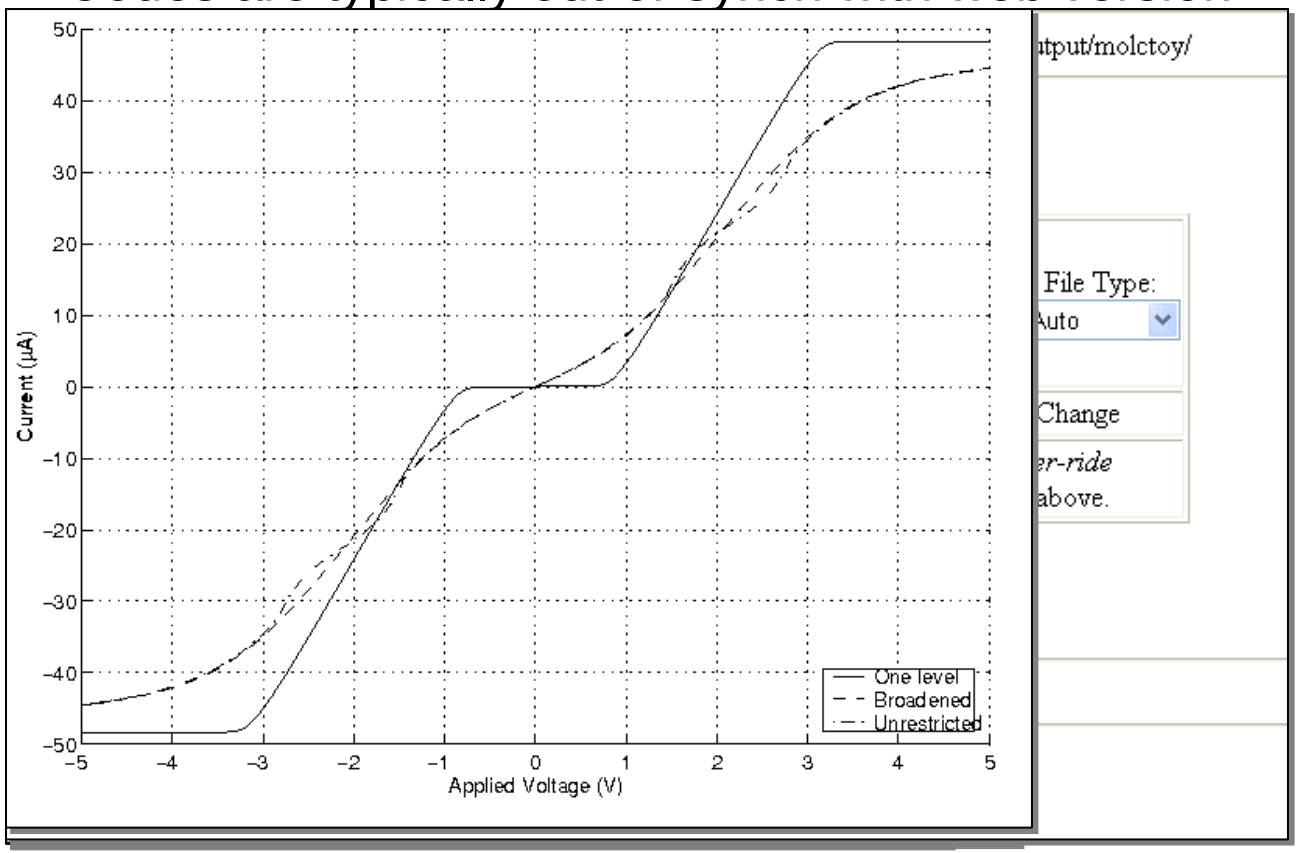


nanoVIS rendering server

Developed by
Wei Qiao, Insoo Woo, David S. Ebert
PURPL Lab, Purdue University

Typical Web-based Simulations

- Started at Purdue 1995 with PUNCH:
  - » Enabled researchers and students to access real simulation codes
  - » traditionally 800 users annually.
- Typical usability is marginal
- Codes are typically out-of-synch with web version



The OLD static GUI

- Form sheet input
- Batch submission
- Output in some file
- Visualize a gif image
- Other output file
- Visualize gif image

Typical Questions:

- What was my input?
- Did I enter things right?

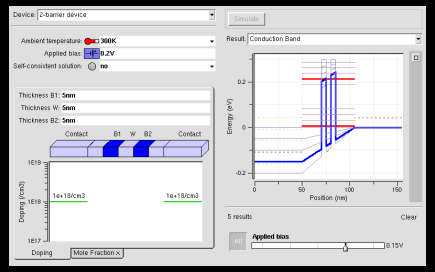
Symptoms of:

- No VISUAL feedback.
- Not interactive.

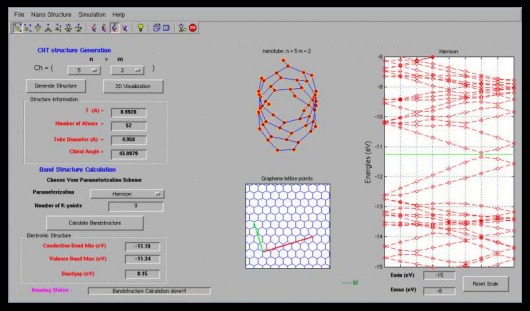
Use in Education

The nanoHUB has proven itself to be an extremely valuable tool for education and research. …We have used the Resonant Tunneling Diode simulator and the MSL simulator on the nanoHUB for homework exercises and mid-term exams. A class survey of the use of the nanoHUB simulation engines had shown that ***the experience is quite positive. The staff at the nanoHUB has been very responsive in supporting our class activities in a professional manner.***

H.-S. Philip Wong
Professor of Electrical Engineering
Stanford University



Resonant Tunneling Diodes



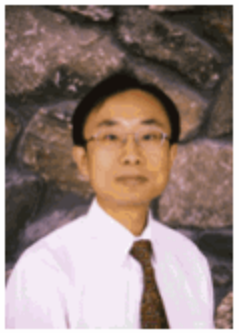
MSL simulator

New Contributor

Contributors

H.-S. Philip Wong

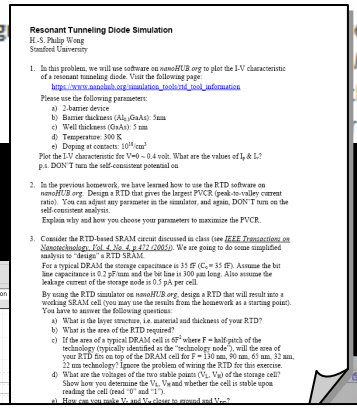
Contributions	2
Affiliation	Stanford University
Web Site	http://www.stanford.edu/~hspwong
Biog	eceived the B.Sc. (Hons.) in 1982 from the University M.S. in 1983 from the State University of New York at he Ph.D. in 1988 from Lehigh University, all in ring. He joined the IBM T. J. Watson Research Center,



H.-S. Philip Wong

Professor of Electrical Engineering

Stanford University



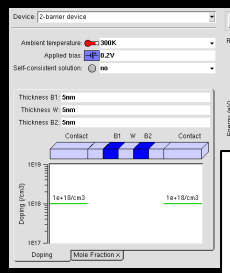
Resonant Tunneling Diode Simulation

H.-S. Philip Wong
Stanford University

1. In this problem, we will use software on *nanoHUB.org* to plot the I-V characteristic of a resonant tunneling diode. Visit the following page:
   https://www.nanohub.org/simulation_tools/rtd_tool_information
   Please use the following parameters:
   a) 2-barrier device
   b) Barrier thickness ($Al_{0.3}GaAs$): 5nm
   c) Well thickness (GaAs): 5 nm
   d) Temperature: 300 K
   e) Doping at contacts: $10^{18}/cm^3$
   Plot the I-V characteristic for V=0 – 0.4 volt. What are the values of I_p & I_v?
   p.s. DON'T turn the self-consistent potential on

2. In the previous homework, we have learned how to use the RTD software on *nanoHUB.org*. Design a RTD that gives the largest PVCR (peak-to-valley current ratio). You can adjust any parameter in the simulator, and again, DON'T turn on the self-consistent analysis.
   Explain why and how you choose your parameters to maximize the PVCR.

3. Consider the RTD-based SRAM circuit discussed in class (see *IEEE Transactions on Nanotechnology, Vol. 4, No. 4, p.472 (2005)*). We are going to do some simplified analysis to "design" a RTD SRAM.
   For a typical DRAM the storage capacitance is 35 fF (C_s = 35 fF). Assume the bit line capacitance is 0.2 pF/mm and the bit line is 300 mm long. Also assume the leakage current of the storage node is 0.5 pA per cell.
   By using the RTD simulator on *nanoHUB.org*, design a RTD that will result into a working SRAM cell (you may use the results from the homework as a starting point). You have to answer the following questions:
   a) What is the layer structure, i.e. material and thickness of your RTD?
   b) What is the area of the RTD required?
   c) If the area of a typical DRAM cell is $6F^2$ where F = half-pitch of the technology (typically identified as the "technology node"), will the area of your RTD fits on top of the DRAM cell for F = 130 nm, 90 nm, 65 nm, 32 nm, 22 nm technology? Ignore the problem of wiring the RTD for this exercise.
   d) What are the voltages of the two stable points (V_1, V_2) of the storage cell? Show how you determine the V_1, V_2 and whether the cell is stable upon reading the cell (read "0" and "1").
   e) How can you make V_1 and V_2 closer to ground and V_{DD}?



Resonant T
Diodes

Homework for Resonant Tunneling Diodes

06 Jan, 2006 | Teaching Materials | Contributor(s): H.-S. Philip Wong

This homework assignment was created by H.-S. Philip Wong for EE 218 "Introduction to Nanoelectronics and Nanotechnology" (Stanford University). It includes a couple of simple "warm up" exercises and two design problems, intended to teach students the electronic properties of resonant tunneling ...

Deji Akinwande

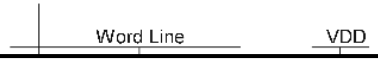
Stanford University

In Philip Wong's Fall 2005 class

A Composite Circuit Model for NDR Devices in Random Access Memory Cells

Deji Akinwande, *Member, IEEE*, and H.-S. Philip Wong, *Fellow, IEEE*

***Abstract*—Devices exhibiting negative differential resistance (NDR), such as resonant tunneling diodes and Esaki-type diodes,**



RTD

er RTD

C. Validation of Composite Model

Analytical models are not useful if they are inaccurate. In Fig. 4, a graphical comparison between the three sets of composite models and experimental composite data from the NDR device reported in [6] are shown. As another example,

[1]Online, available http://www.nanohub.org, "Resonant tunneling diodes simulator." The "self-consistent solution" option was turned off. Contact/well material = GaAs, barrier material = AlAs, contact doping = $1 \times 10^{19}/\text{cm}^3$, barrier width = 1 nm, well width = 1.5 nm, RTD area = 918 nm^2.

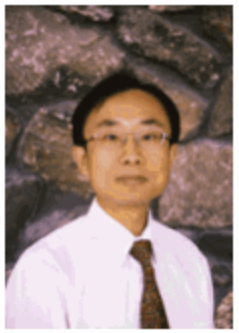
More Contributions

Contributors

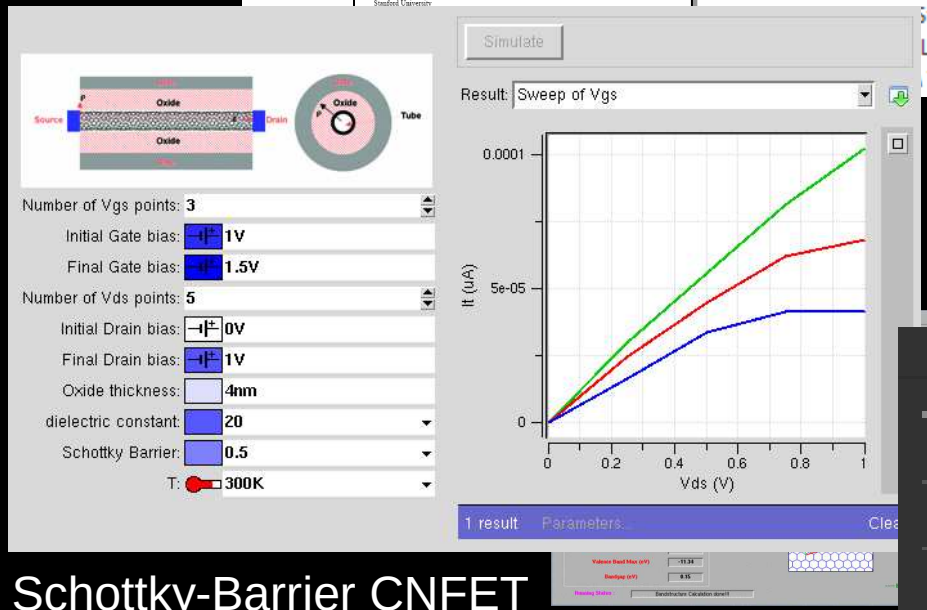
H.-S. Philip Wong

Contributions	2
Affiliation	Stanford University
Web Site	http://www.stanford.edu/~hspwong

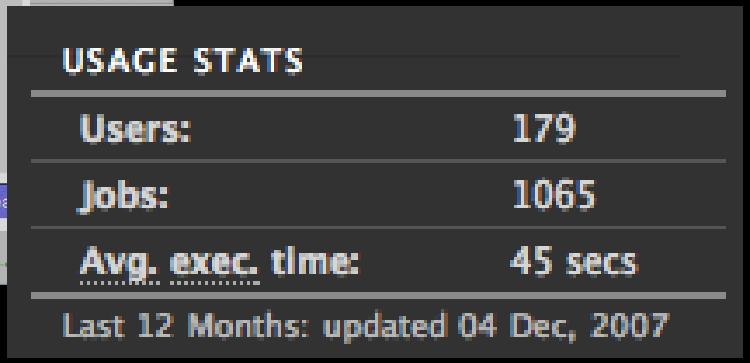
Biog Resonant Tunneling Diode Simulation H.-S. Philip Wong Stanford University eceived the B.Sc. (Hons.) in 1982 from the University tate University of New York at Lehigh University, all in T. J. Watson Research Center,



H.-S. Philip Wong
Professor of Electrical Engineering
Stanford University



Schottky-Barrier CNFET
Online March 16, 2007



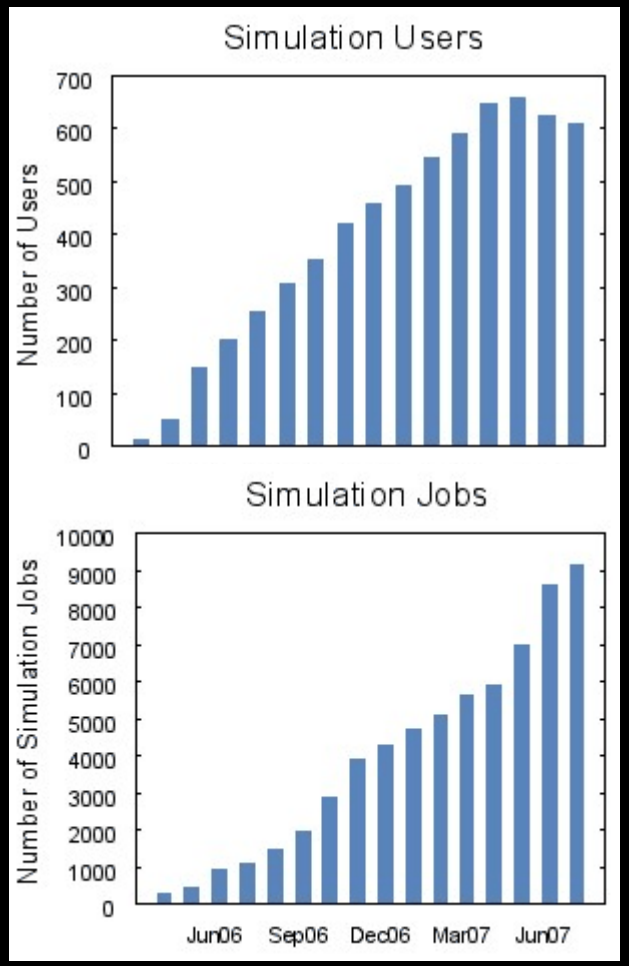
nanowire

Usage Statistics

Released May 19, 2006

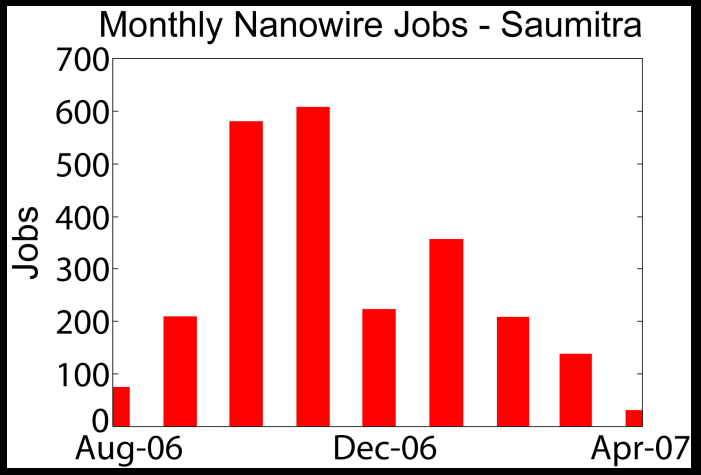
610 Users

9,115 Simulations



Saumitra Mehrotra

Univ. of Cincinnati



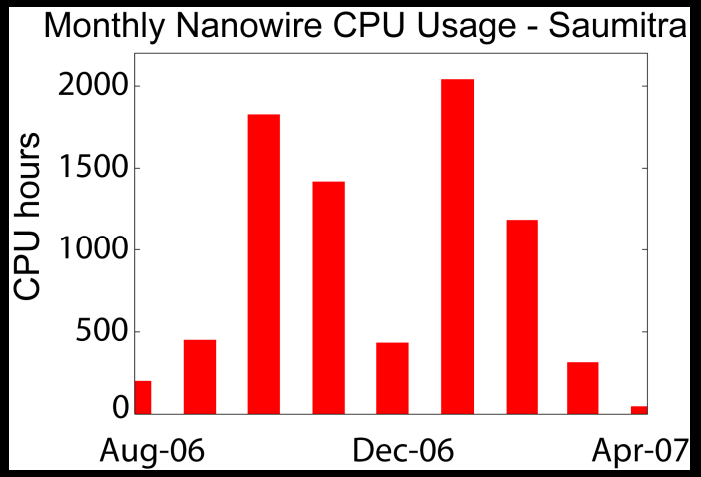
In the past 10 months:

26 tools / 3,327 simulations

- 47 simulations: bandstructure lab
- 240 simulations: FETtoy
- 2,855 simulations: nanowire
- 8,242 nanowire CPU hours

- “and more” content
  134 items, 52 hours

- 96 support tickets
  69 entered manually,
  27 filed automatically by application



IEEE Workshop on Microelectronics and Electron Devices (WMED), April 20 2007

Process Variation Study for Silicon

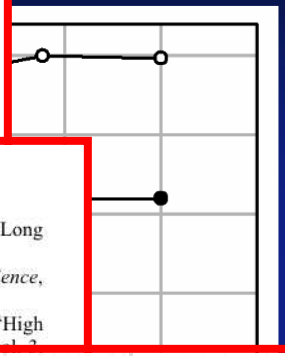
Simulation Tool

SiNW FET Vs FinFET – Gate Length Variation

Process Variation Study for Silicon Nanowire Transistors

performance in circuits and superior reproducibility for the SiNW FETs.

Fig. 4 shows the variation in the threshold voltage with change in the gate dielectric thickness. Again, the SiNW FET shows a smaller variation (1.2 mV/A) compared with the FinFET's 5 mV/A. Also of interest is the sensitivity of the devices to the gate length. Shown in Fig. 5 is the threshold



REFERENCES

[1] W.S.Shi et al., "Synthesis of Large Areas of Highly Oriented, Very Long Silicon Nanowires," *Adv. Mater.* 12, 1343, 2000.

[2] D. Ma et al.," Small-Diameter Silicon Nanowire Surfaces," *Science*, 299, p. 1874, 2003.

[3] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High

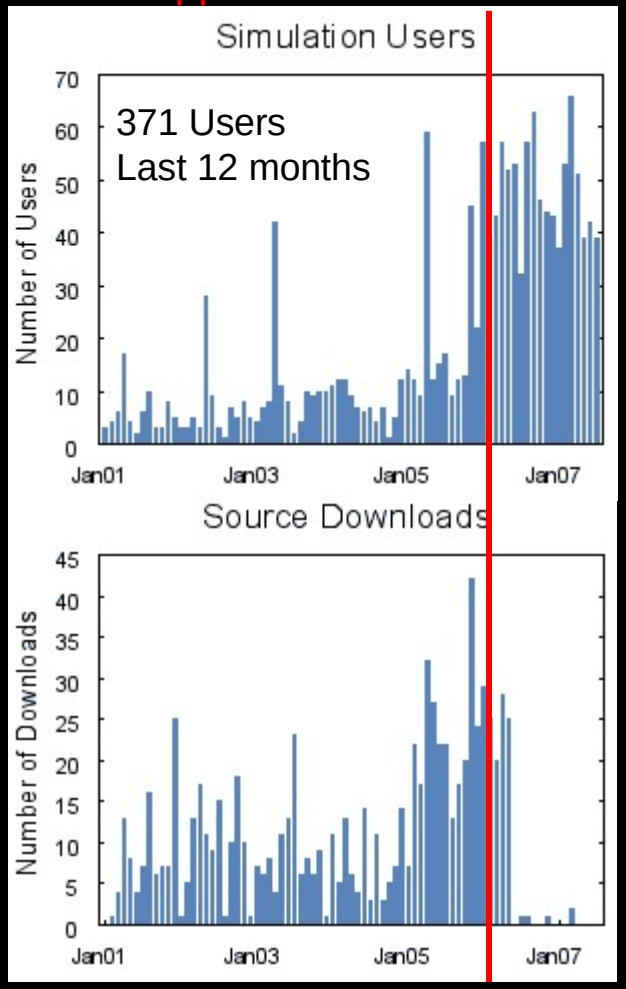
[7] J. Wang, E. Polizzi, M. Lundstrom, "A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation," *Journal of Applied Physics* **96**(4), pp. 2192-2203, 2004.

[8] Simulations were performed on http://nanohub.org

[9] J. Wang, E. Polizzi, and M. Lundstrom, "A computational study of ballistic silicon nanowire transistors," in *IEDM Tech. Dig.*, Dec. 8–10, 2003,pp. 695–698.

Case in point

Rappture version Feb 06



TCAD simulations using SCHRED [15] or ISE, …., were used to support our analysis and compute the inversion carrier profiles in the devices.

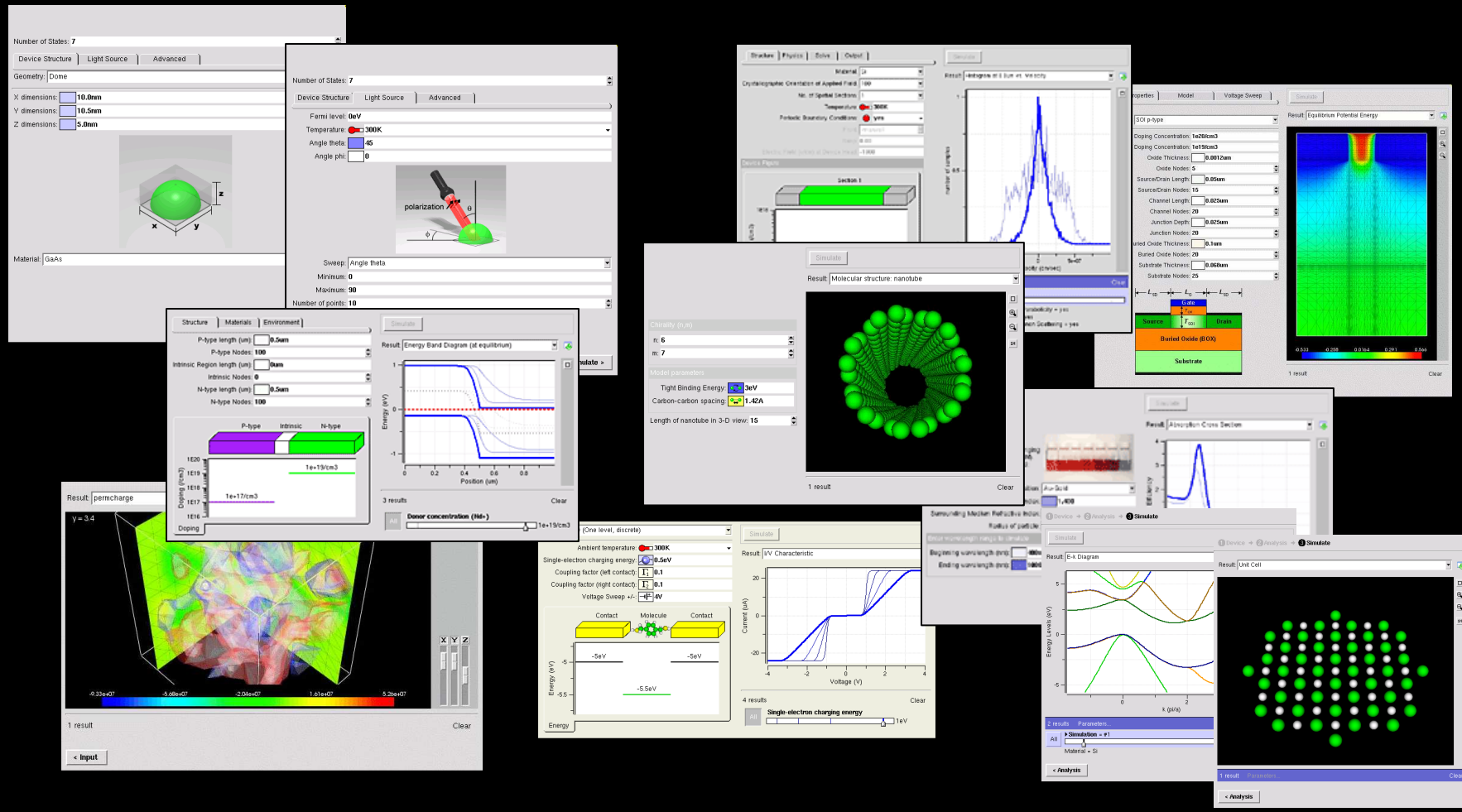
Effect of channel positioning on the 1⁄f noise in silicon-on-insulator metal-oxide-semiconductor

M von Haartman, M Oestling,
Journal of Applied Physics, 2007 - link.aip.org**...**

- Same behavior across all similar converted tools
- User's don't have to download/install software

Over 50 tools online!

50 more in the pipeline



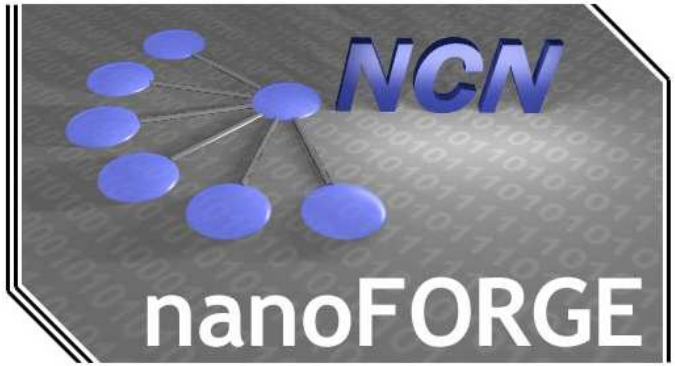
nanoFORGE.org

Open-source AND closed-source code development

>120 projects

Welcome to nanoFORGE, the project development area of nanoHUB.org. The following pages are maintained by the various owners of each project. Many of these tools are available as Open Source, and you can download the code via Subversion from this site. Some tools are closed source at the request of the authors, and only a restricted development team has access to the code. See each project page for details.

Become a member! Sign up for a free nanoHUB account and use this site to manage your software project.



Infrastructure Projects

- hubzero
- lib-gangli
- nanohub
- nanohub-for-kids
- nanohub-support
- ncn
- ncn_students
- nmi
- pharmengine
- rappture
- rappture-runtime
- rkspack
- sysman
- xhub

Applications

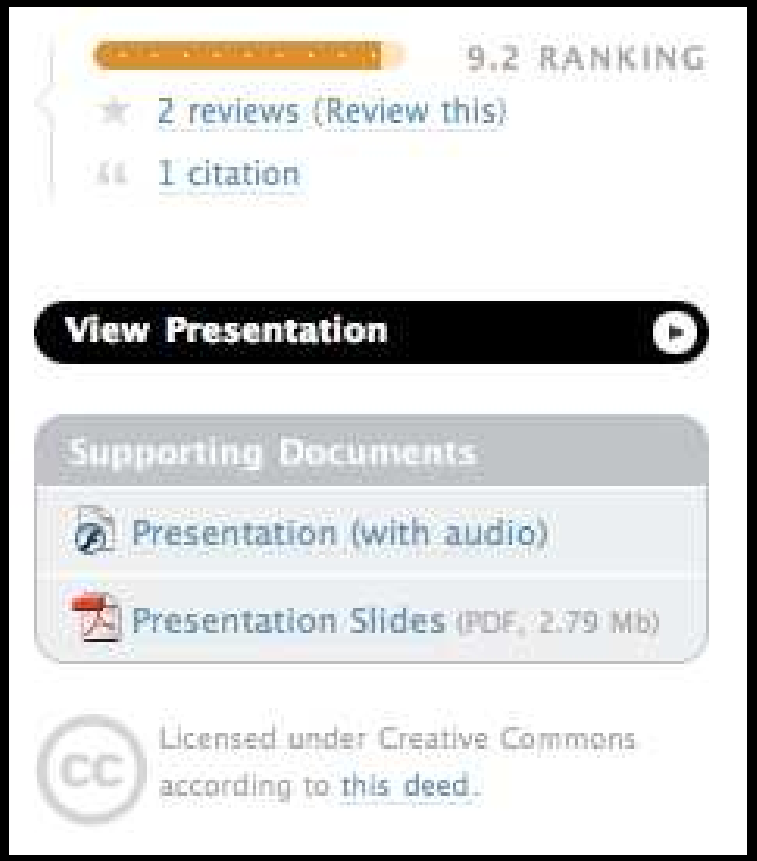
- app-abinit
- app-adept
- app-bandstrlab
- app-beamprop
- app-biomoca
- app-biomolelab
- app-biophet
- app-biotrpnp
- app-blast
- app-brownianmotion
- app-bstr_sc_lab
- app-cacti
- app-cenems
- app-cgtb
- app-chemkinetics
- app-chess
- app-cndo

825 resources

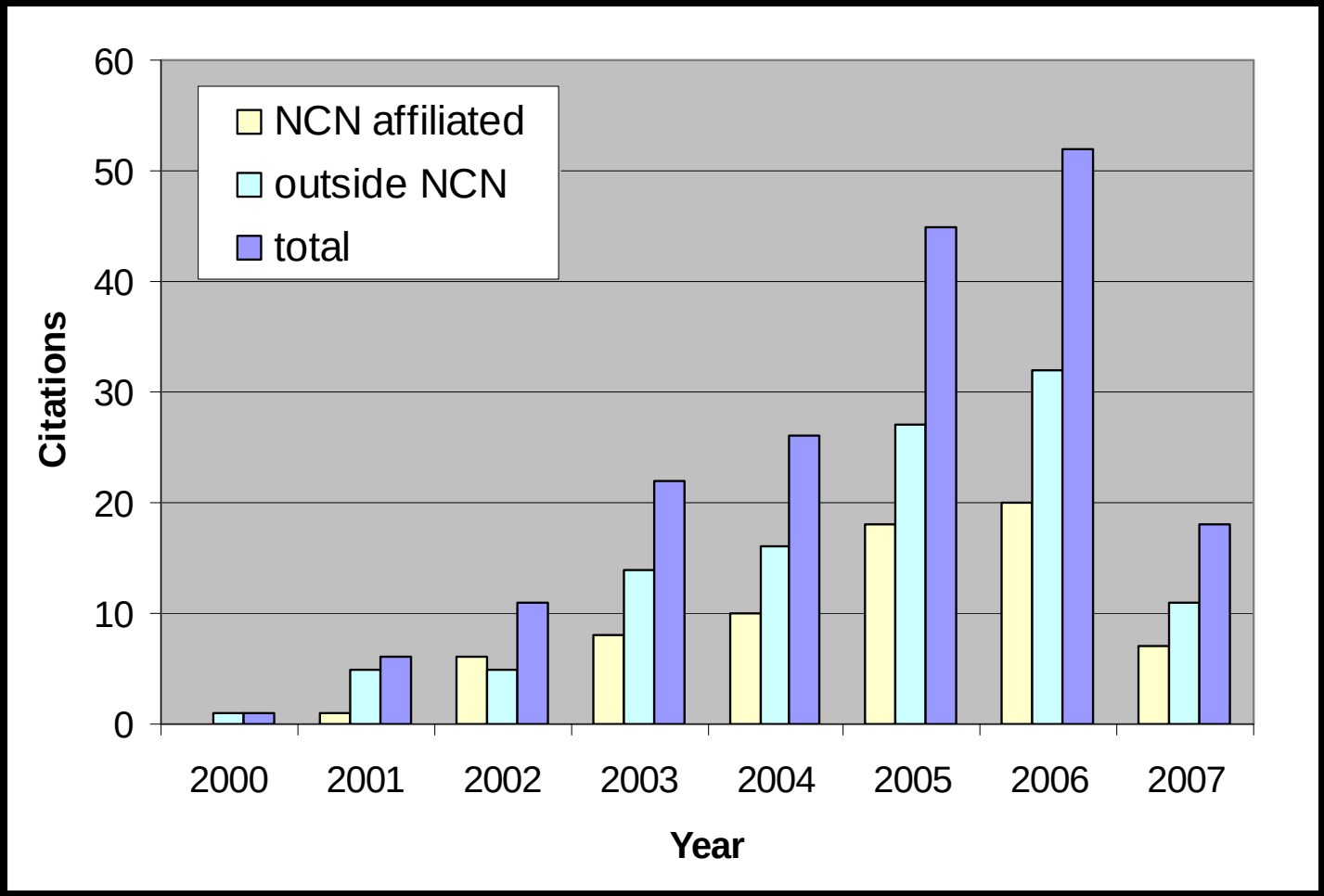
279 added
Nov 06-Oct07

Most licenses:

Creative Commons



nanoHUB Citations



187
total

114
60%
non-NCN

Who's using this?

>3 million hits last month

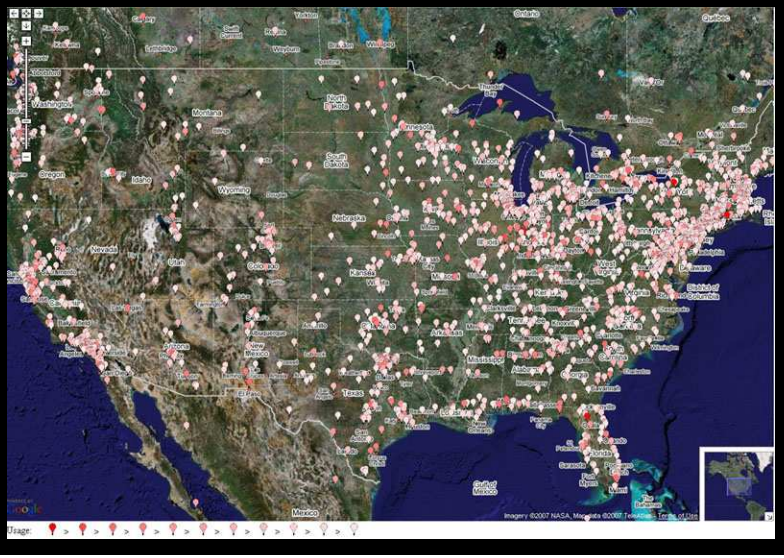
>1 million visits last 12 months

26,597 users last 12 months

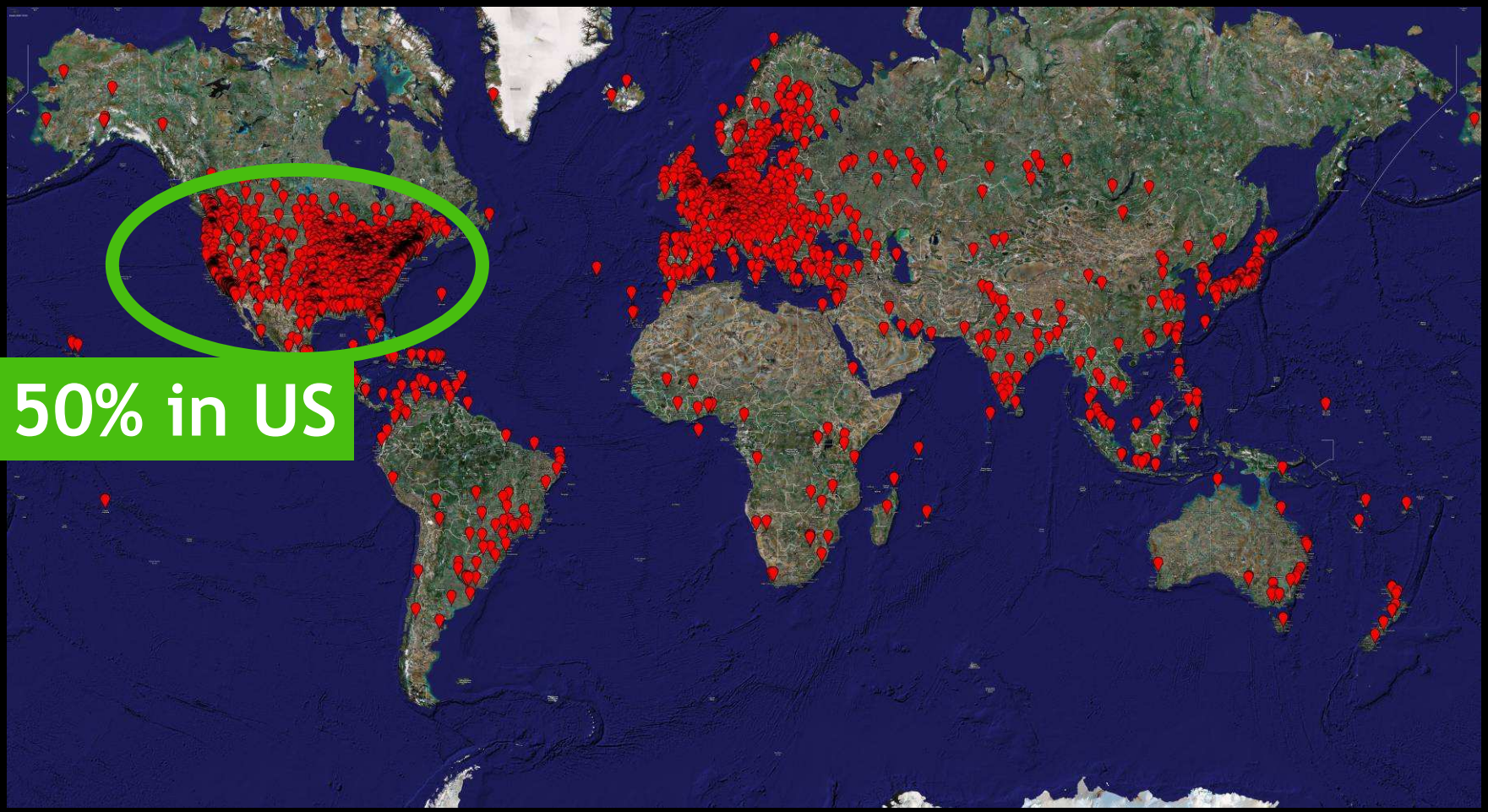
218,656 simulation jobs last 12 months

51 of the Top 50 Engineering Schools

11.75% of all .edu domains



A global following



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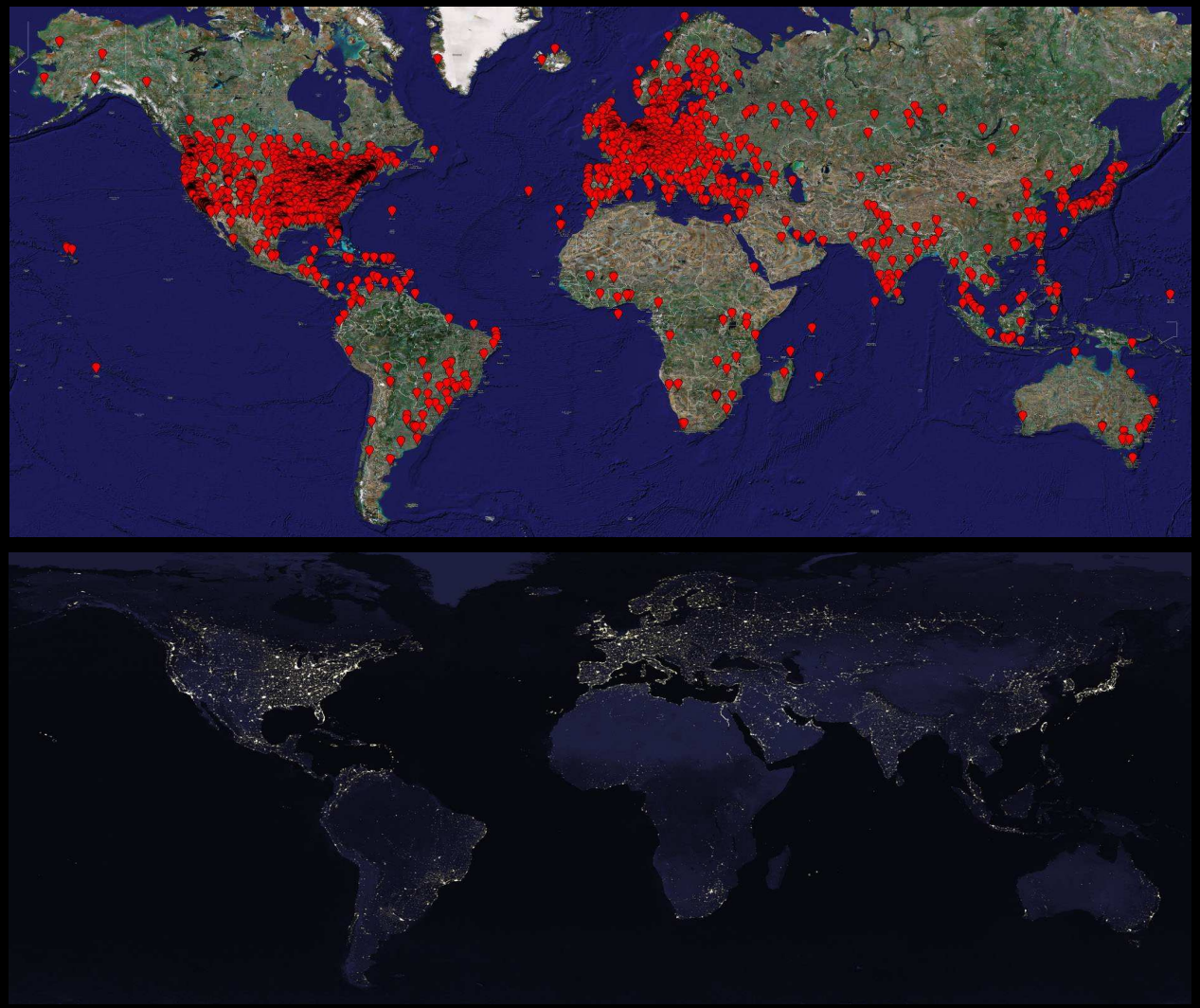
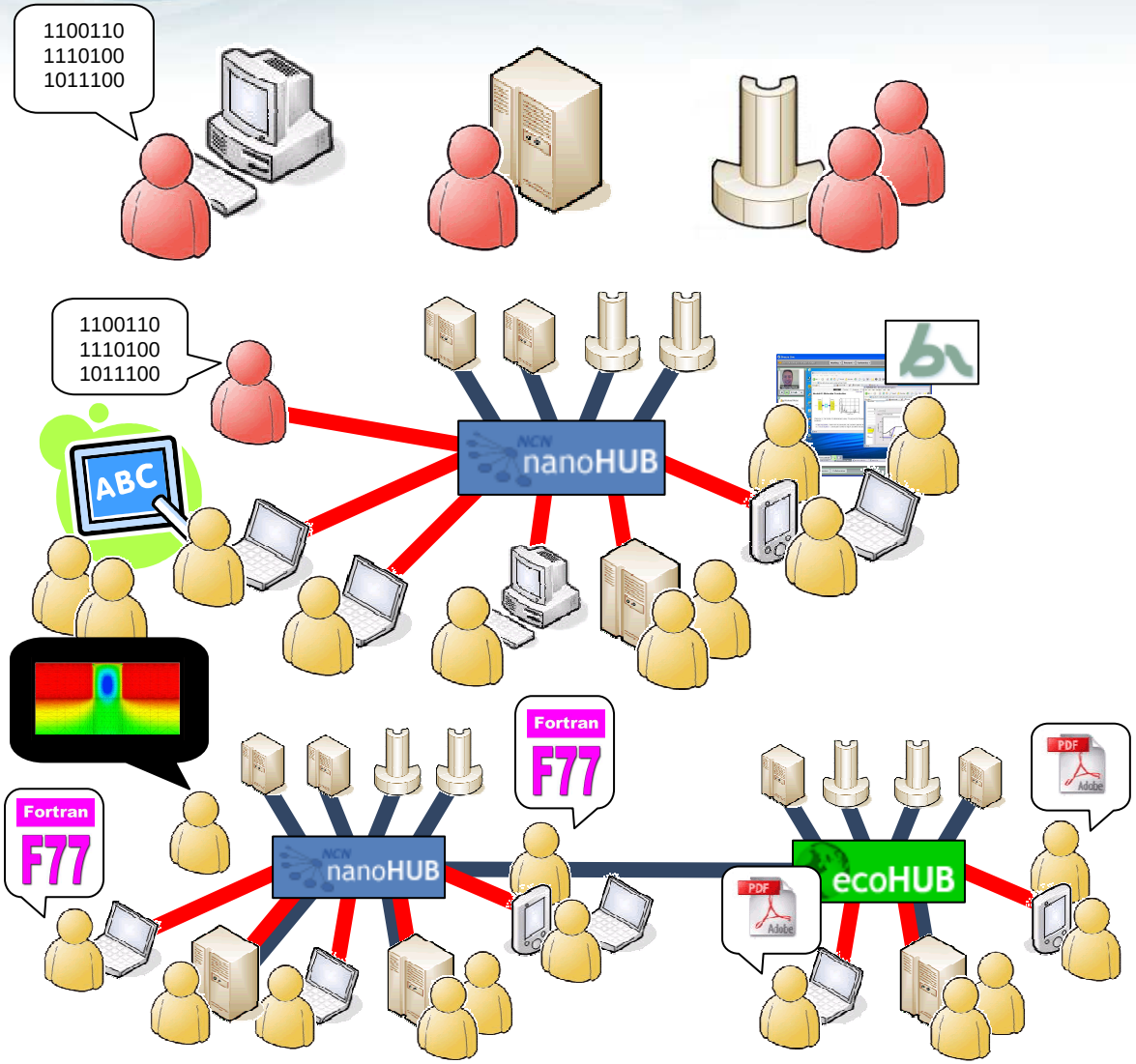


nanoHUB online simulation and more — an NCN project

Evolution of Scientific Computing



Scientific & HPC Computing

few users with specialized knowledge

Science Gateways

cyberinfrastructure, more users

Cyber Communities

ecosystem, users support each other

6 other HUBs Under Development

nanohub.org – Mark Lundstrum, ECE at Purdue
the granddaddy of all hubs focused on nanotechnology
online since 2002, PUNCH online since 1995

IndianaCTSI.org – Anantha Shekhar,
IU School of Medicine
accelerating clinical and translational research in healthcare
online since 10/1/2007

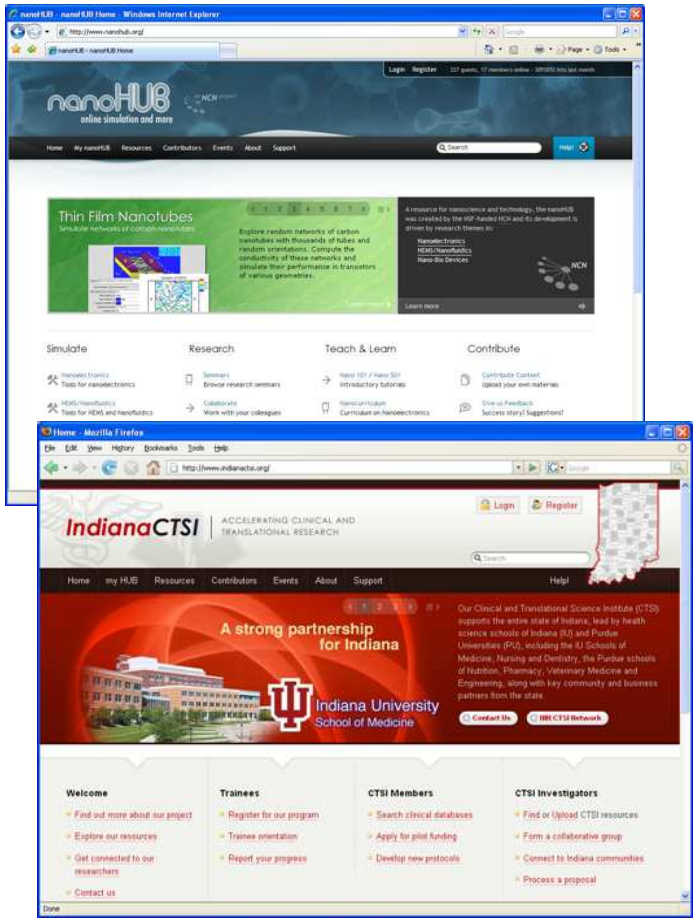
pharmaHUB.org – Rex Reklaitis, CE at Purdue
pharmaceutical product development and manufacturing
coming online by 11/30/2007

thermalHUB.org – Tim Fisher, ME at Purdue
heat transfer
coming online by 11/30/2007

globalHUB.org – Dan Hirleman, ME at Purdue
global engineering education
coming online by 12/17/2007

manufactureHUB.org –Shade, IE at Purdue
manufacturing engineering
coming online by 2/28/2008

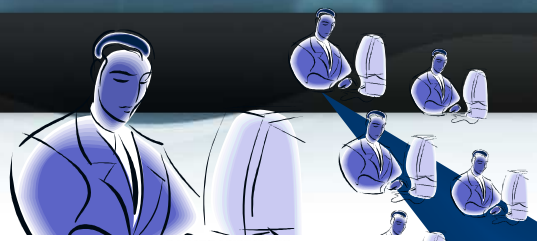
cancerHUB.org – Nagle, DP Purdue
cancer care (tools built now, online 2009)

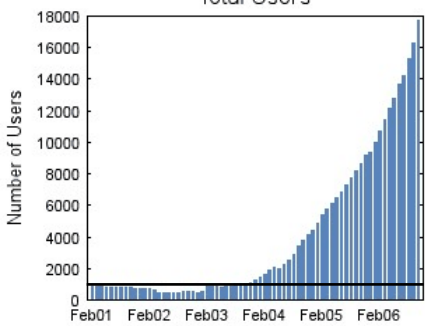


PURDUE UNIVERSITY ITaP NCN

nanoHUB
online simulation and more
an NCN project

Online simulation and more

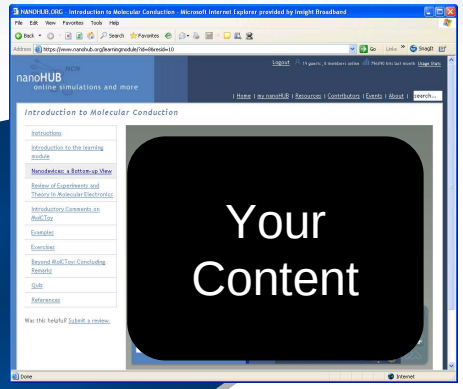




Real users and real usage
>26,000 users

collaboration

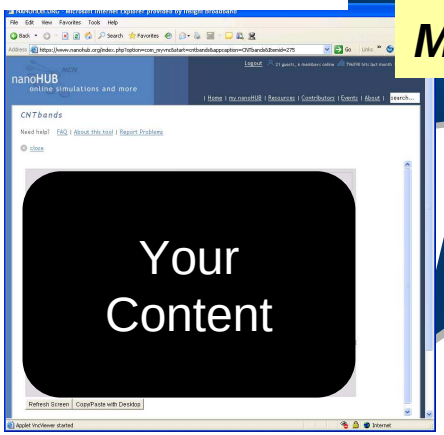
learning modules



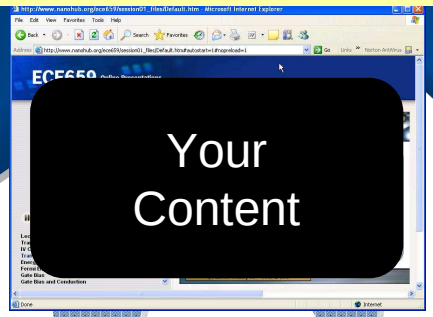
Become an uploader

nanoHUB.org

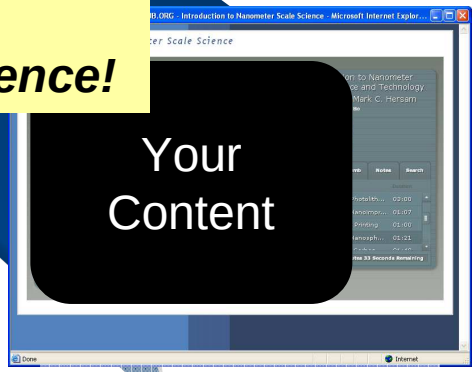
Outreach:
Make IMPACT with your Science!



online simulation



courses, tutorials



seminars

PURDUE UNIVERSITY Gerhard Klimeck

NCN NSF