Atom-Scale Silicon Integrated Circuits for Quantum Computation

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T.-C. Shen[1], J. R. Tucker[2], J. Bokor[3], T. P. Ma[4], and R. R. Du[5]
[1]Utah State University, [2]University of Illinois, [3]University of California at Berkeley,
[4]Yale University, [5]University of Utah

The goals and impact

One of the most important goals for nanotechnology is to realize a post-roadmap electronics. A myriad of proposals have been put forward in this direction, from molecules and nanotubes to cellular automata and quantum computers, but one thing seems certain-nearly all of these concepts will need to be integrated with conventional silicon electronics in order to become practical. The goals of this project is to extend conventional silicon technology to atomic dimensions: to control single spins and single charges in conventional materials, to study electron transport at that scale, and to develop the basic components for a silicon-based quantum computer. Specifically at the device level we plan to use patterned 2-dimensional dopant sheet as building blocks for field effect transistors and single electron transistors. At the system level, we plan to demonstrate that dopant devices can be integrated with conventional CMOS circuits and large scale integrated circuits made entirely of donors and acceptors are possible by existing technologies. Our long-term goal is to develop a flexible silicon-based process capable of exploring a wide range of new possibilities relevant to information processing.

The approach

At sufficient high dopant concentration, silicon can be metallic. Polysilicon gate and the source/drain regions in the conventional metal-oxide-semiconductor-field-effect-transistor (MOSFET) are common examples. However, conventional doping techniques, such as diffusion or implantation, cannot control the dopant distribution to the atomic scale. Hence it would be difficult to define nanoscale dopant circuits that way. The key advantages of our approach are: (1) employing hydrogen resist in ultrahigh vacuum allows low-energy e-beam lithography to achieve atom-scale resolution; (2) selective adsorption of dopant atoms onto the patterned region by precursor gas molecules such as PH_3 or B_2H_6 avoids dopant clustering and high temperature activation annealing; (3) low-temperature epitaxial silicon overgrowth after precursor adsorption reduces dopant diffusion and activates dopant; (5) epitaxial silicon tunnel junctions can suppress both the telegraph noise and the random polarization offsets of single electron transistors to very low levels allowing large scale integration; and (6) the epitaxial device structures open the door for 3-dimensional architectures. [2]

The collaboration

The 2-terminal device templates were designed, fabricated and characterized by Prof. Tucker's group. The contact in the templates were either As or Ga implanted. Prof. Shen's group developed a low-temperature surface cleaning process in ultrahigh vacuum, where atomically clean and flat surfaces can be achieved on the pre-implanted device templates. STM e-beam lithography, phosphine adsorption and Si overlayer growth were conducted in Prof. Shen's ultrahigh vacuum system. The samples were sent to Prof. Ma's laboratory to deposit a layer of silicon nitride at room temperature by jet vapors. The finished devices were sent to Prof. Du to characterize the device performance at cryogenic temperatures. Prof. Bokor's group has

developed a new 4-terminal device template and will work closely with Prof. Shen to develop a process allowing integration of nanometer dopant devices with conventional MOSFET.

The results

We have established earlier that a single layer phosphine adsorbed on Si(100) surfaces creates an ultra-dense (~1×10^{14} cm^{-2}) 2-dimensional electron gas (2DEG) in silicon.[3] This novel 2DEG shows no freeze-out and negative magnetoresistance at 0.3 K, a characteristic of 2-dimensional disordered metal.

Recently we have fabricated many P-dopant wires on our 2-terminal templates.[4] The width of the wires ranges from 5 to 95 nm. A 33-nm wire patterned on a H-resist is shown in Fig. 1. The P-donor devices were fabricated across the 1 μm gap between two As implanted interdigitated lines of the templates (Fig. 2).

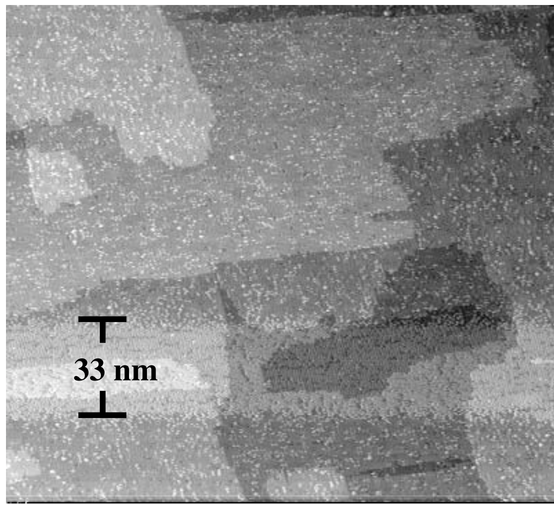

Fig. 1 A 33 nm-wide line H-desorption pattern ready for phosphine adsorption.

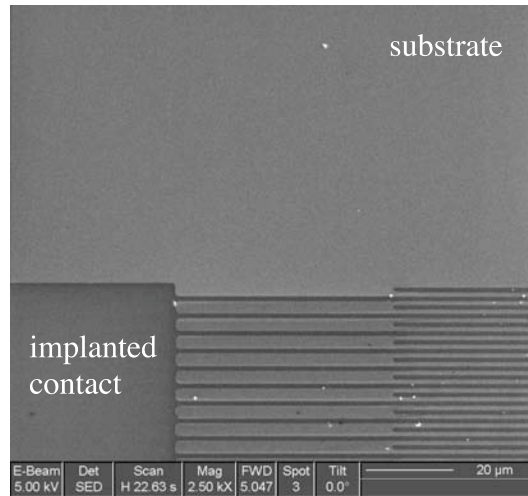

Fig. 2 As ion implanted two-terminal template. Device region is between any two interdigitated lines at lower right.

The I-V characteristics of a set of 200, 95 and 50 nm wide wires (all 1 μm long) at 0.3 K are shown in Fig. 3. The linear relations demonstrate ohmic contact between the P-donor wires and the As ion implanted contacts. The P-donor wires conduct metallically at cryogenic temperatures, indicating total wavefunction overlapping of all donor atoms. The sheet resistance, after correction of the contact contribution, is between 4.3 and 8.6 ohm per square. Magnetoresistance measured at 0.3 K in a perpendicular magnetic field can be fitted into standard 2-dimensional weak localization theory of 2-D disordered metal. The black curve in fig. 4 is the experimental data while the red curve is a fitting, from which one can extract the phase coherence length of a 50 nm wide P-donor wire being 22 nm and the physical width 34 nm. Thinner wires (< 30 nm) occasionally show non-linear I-V characteristics and oscillatory magnetoresistance suggesting quantum interference effects. The underlying physics is currently under investigation.

Currently we have fabricated tunnel junctions as shown in Fig.5 and a new 4-terminal device template (Fig. 6). Together with a JVD nitride layer and metal gate, we are ready to explore 40 nm field effect transistors and all-epitaxial silicon-based single electron transistors.

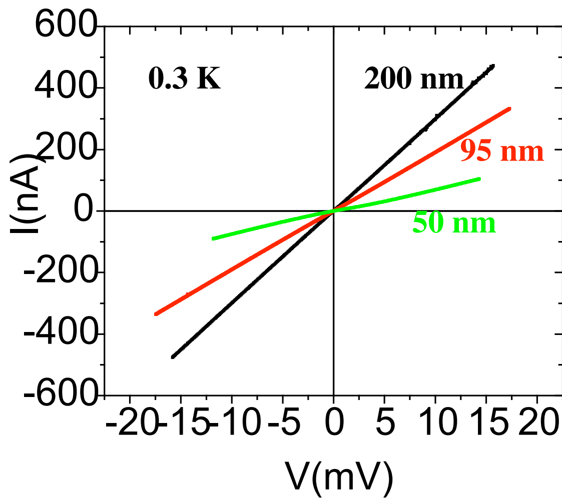

Fig. 3 I-V characteristics of 1 μm long P-donor wires of various widths at 0.3 K.

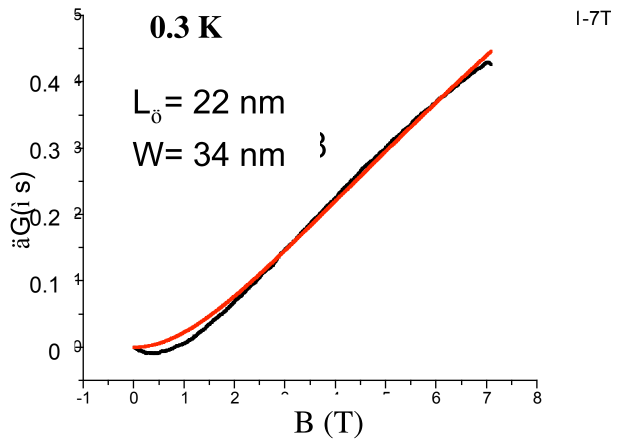

Fig. 4 Magnetoresistance of 50 nm wide P-donor wires. Red curve is a fitting.

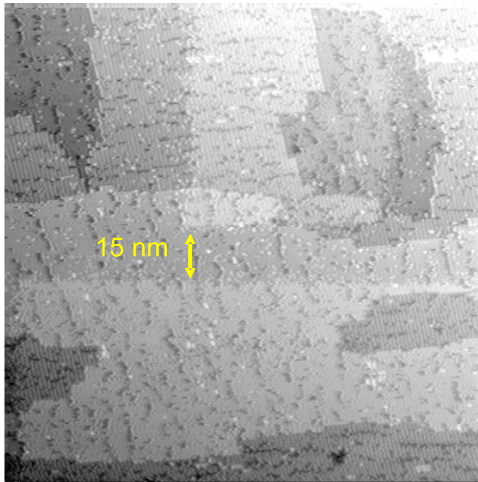

Fig. 5 Lithography of a 15 nm tunnel junctions on H-resist.

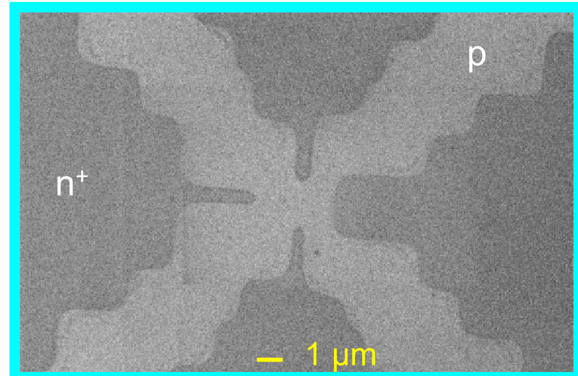

Fig. 6 A 4-terminal device template. The n+ region is As ion implanted.

References

[1] For further information about this project email **<tcshen@cc.usu.edu>**

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