New Devices and Architectures for Energy Efficient Computing

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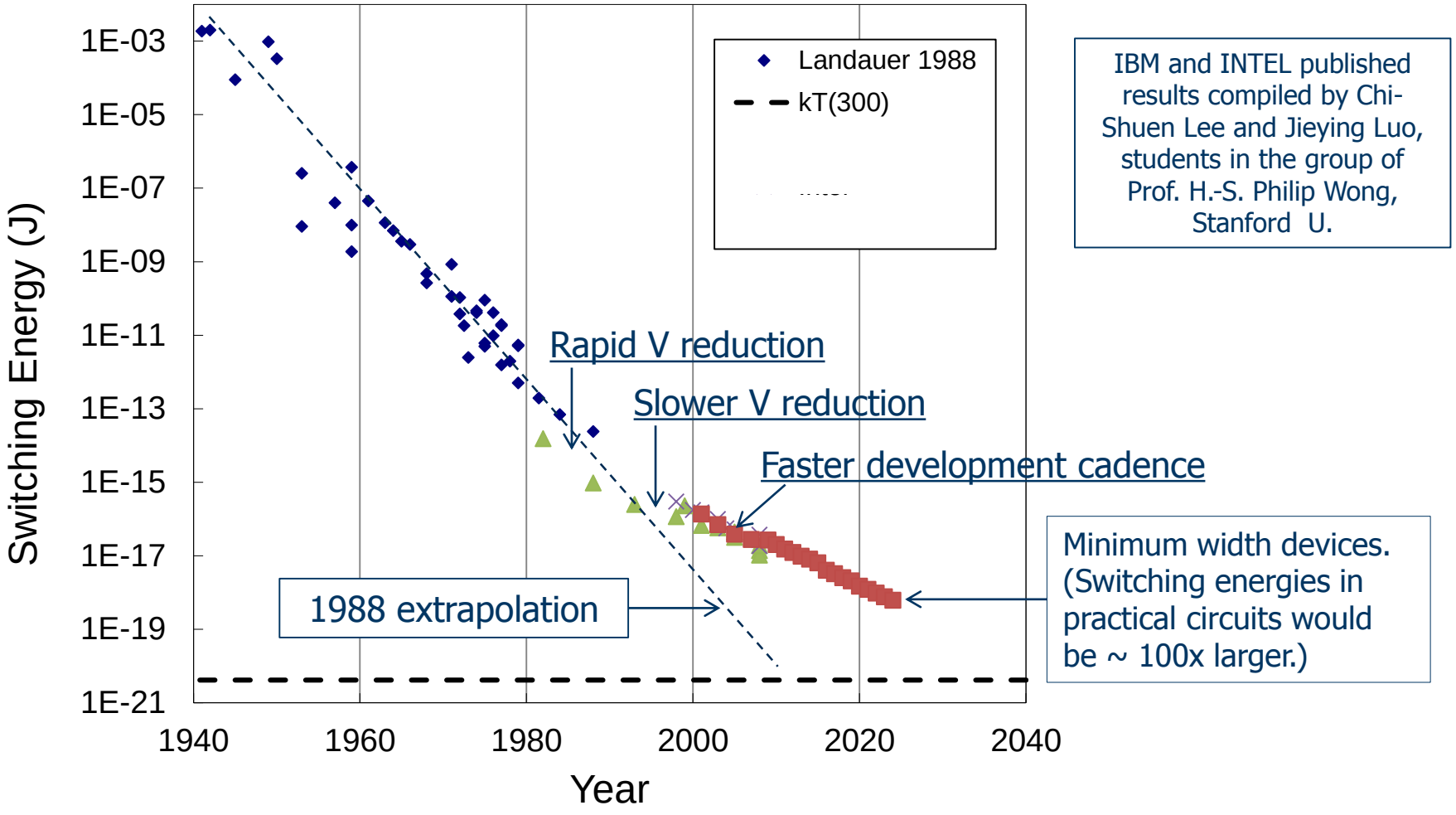
Focusing on Energy Efficient Computing

- National Strategic Computing Initiative
  Strategic Goal 3: Establishing, over the next 15 years, a viable path forward for future HPC systems even after the limits of current semiconductor technology are reached (the "post-Moore's Law era")

- Rebooting the IT Revolution: A Call for Action
  (NSF, Semiconductor Industry Association, Semiconductor Research Corp.)
  Critical Research Challenge 1: Energy Efficient Sensing and Computing

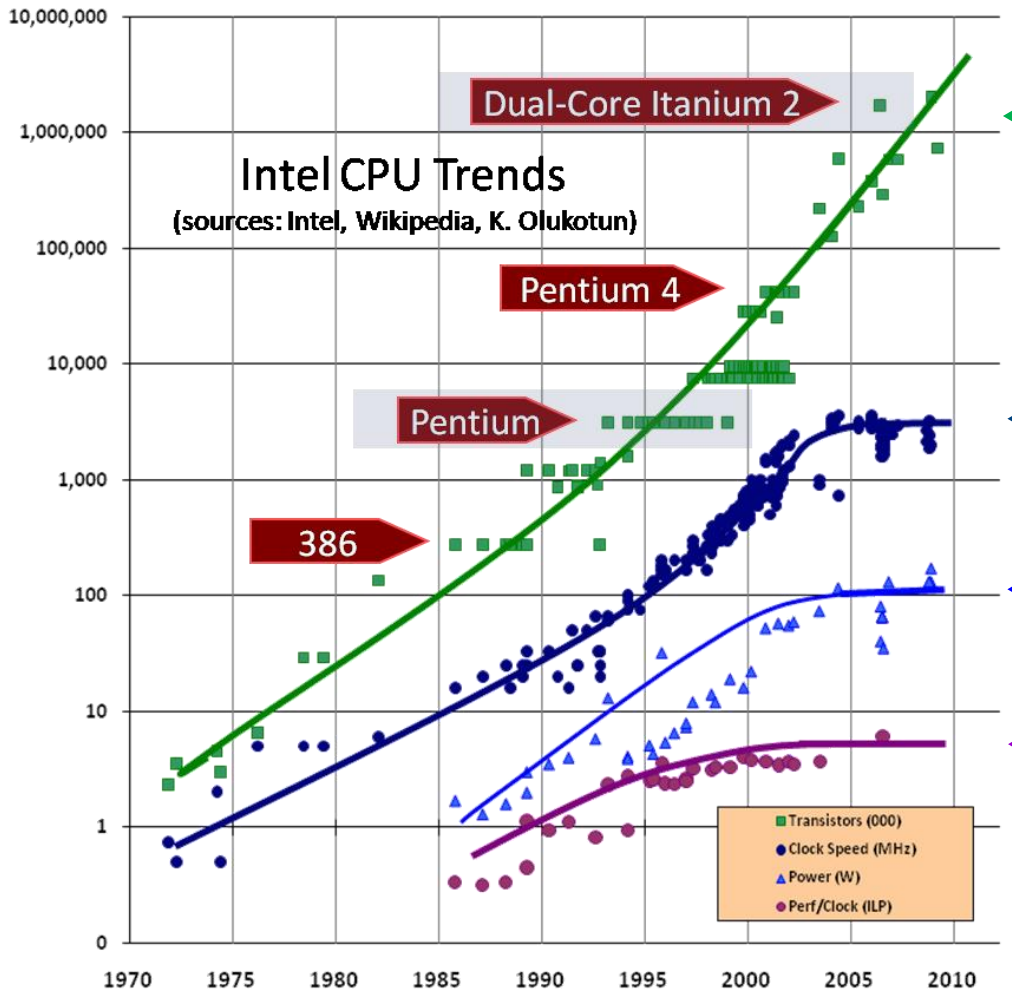
- A Nanotechology-Inspired Grand Challenge in Future Computing
  Create a new type of computer that can proactively interpret and learn from data, solve unfamiliar problems using what it has learned, and operate with the energy efficiency of the human brain.

Minimum Switching Energy for Logic: A Long View



T.N. Theis and H.-S. P. Wong, Computing in Science and Engineering, to be published.

Computer clock frequencies have been stagnant since 2003.



Transistor Count
(still growing)

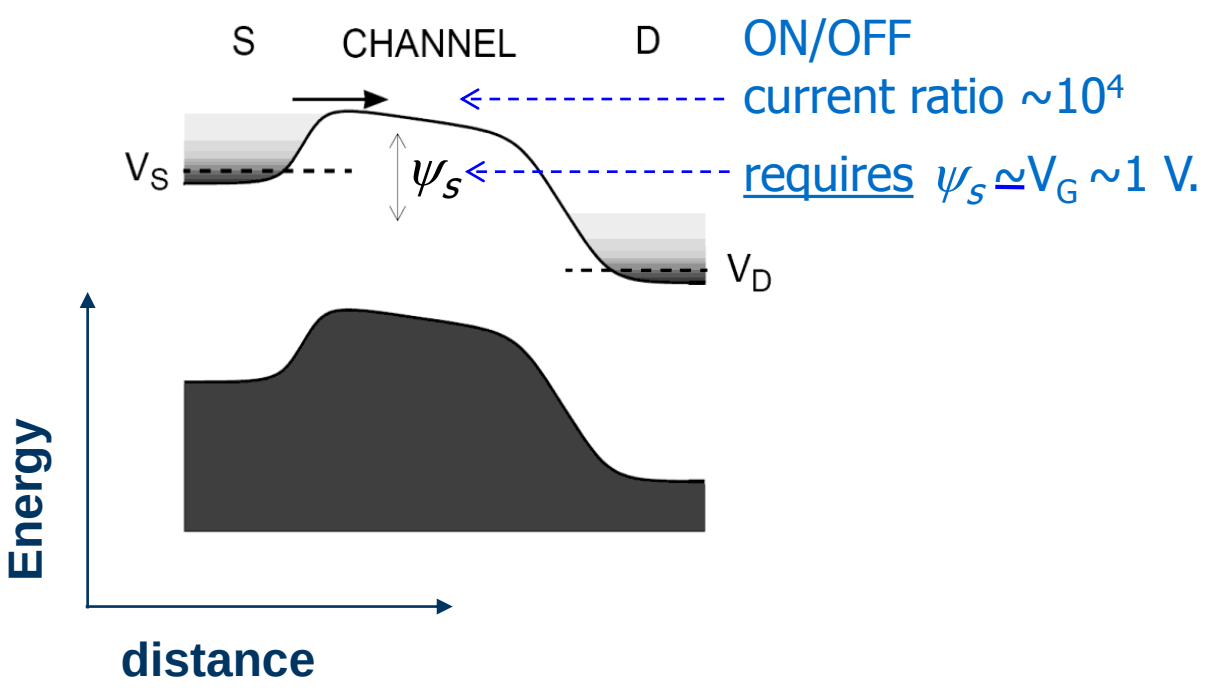
Clock Frequency
(flat since 2003)

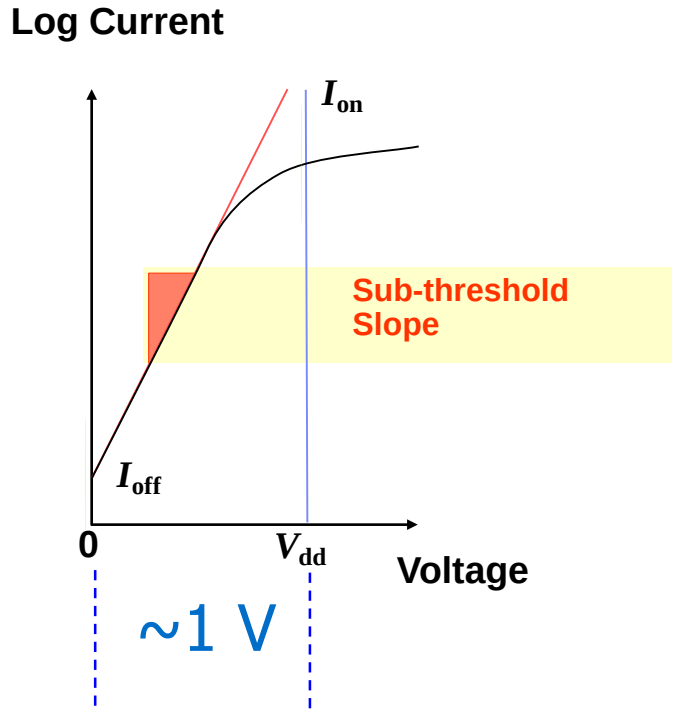
Power
(flat since 2003)

Architectural Innovation (ILP)
(also flagging!)

http://www.gotw.ca/publications/concurrency-ddj.htm

Transistor operating voltage can no longer be reduced along with device dimensions.





With voltage swing already reduced to ~ 1V, The FET is close to its fundamental voltage limit for operation at ambient temperatures.

Briefly summarizing the last 10 years…

- To keep areal power density and total power within economically acceptable limits, industry froze clock speed and slowed the deployment of multiple cores.
  (See the simple constant voltage scaling argument by T.N. Theis and P.M. Solomon, "In Quest of the 'Next Switch': Prospects for Greatly Reduced Power Dissipation in a Successor to the Silicon Field-Effect Transistor," IEEE Proc. 98, 2005–2014, Dec. 2010.)

- To escape this new status quo, we've begun to explore devices with switching mechanisms that are fundamentally different from that of the conventional FET, and architectures than are fundamentally different from the von Neumann architecture.

Growing Research Investments in New Devices and Architectures for Computing

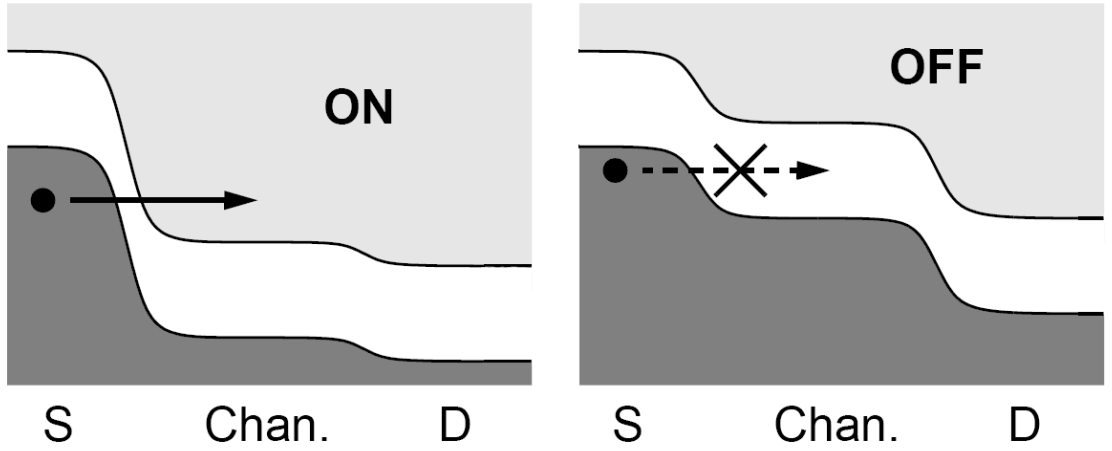
Research funded by industry and government (NSF, NIST, DARPA) in recent years has given us a broader picture of what is possible.

- Founded in 2005, the Nanoelectronics Research Initiative (NRI) is a public-private partnership funding university research aimed at demonstrating *non-conventional, low-energy technologies for computation which can outperform CMOS on critical applications in ten years and beyond.*
- In 2013, NRI was joined in the focused exploration of post-CMOS devices by the former Focus Center Research Program, completely refreshed as STARnet.
- 3 NRI and 3 STARnet multidisciplinary, multi-university research centers are currently exploring a wide range of emerging device concepts, and stimulating additional research and invention by others. 3 other STARnet centers are exploring new architectures for computing.

“Steep Slope” Devices

How long does it take to truly understand the potential of a promising device concept?

Let's consider today's most-studied emerging device – the Band-to-Band Tunneling Field Effect Transistor or TFET



A Very Brief History of TFET Research

- 1989: First report of gated tunneling
  S. Banerjee *et al.,* IEEE Electron Device Lett. **EDL-8**, pp. 347–349, Aug. 1987.
- 2005: SS less than 60 mV/decade in CNT TFET
  Appenzeller, *et al.*, Phys. Rev. Lett. **93**, art. 196805, Nov. 2004.
- 2007: DARPA STEEP program focuses on Si and Si-Ge TFETs
- 2009: III-V broken-gap heterojunction TFET proposed (NRI MIND Center)
  S. O. Koswatta *et al.*, IEDM 2009.
- 2013: Prediction of new ultra-low power design space opened by TFETs
  U. Avci and I. Young, IEDM 2013.
- Current:
  - New TFET variants continue to emerge
    (i.e. graded composition nitrides; P. Fay *et al.*, *STARNET LEAST Center)*
  - But subthreshold slope in high-current (fast switching) devices continues to disappoint, and the fundamental leakage mechanisms that may explain this are still poorly understood.

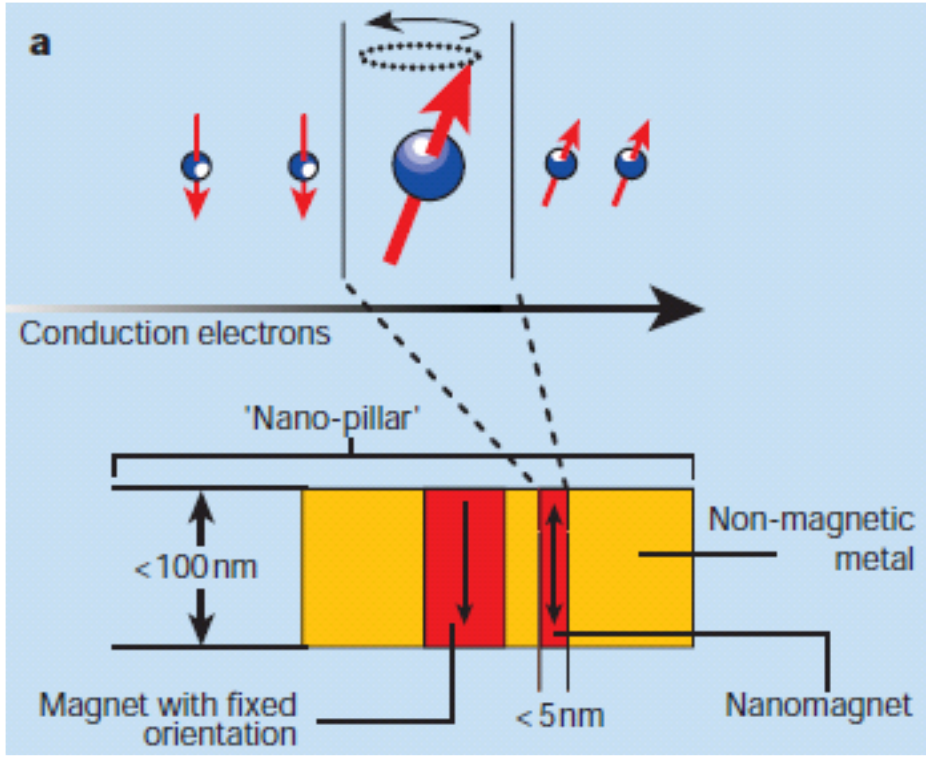
Newer steep slope device concepts continue to emerge.

- Negative Capacitance FET
  S. Salahuddin and S. Datta, Nano Lett., vol. 8, no. 2, pp 405–410, December 2007.
- Graphene p-n Junction (GPNJ) Device
  NRI INDEX center
  R.N. Sajjad and A. W. Gosh, arXiv:1305.7171, May 2013.
- Piezoelectronic Transistor (PET; solid-state relay)
  D.M. Newns, B.G. Elmegreen, X.-H. Liu and G.J. Martyna, J. Appl. Phys., vol. 111, art. 084509, 2012.
- PiezoFET
  STARnet LEAST center
  R. K. Jana, G. L. Snider, and D. Jena, *physica status solidi (c)*, vol. 10, no. 11, pp. 1469-1472, November 2013.
- and more …

Nanomagnetic Devices

Modifying magnetization by spin currents

- Current, when passing through a ferromagnet, becomes spin-polarized.
- Conduction electron spins exert a torque on magnetic moments: Spin-transfer torque (STT).



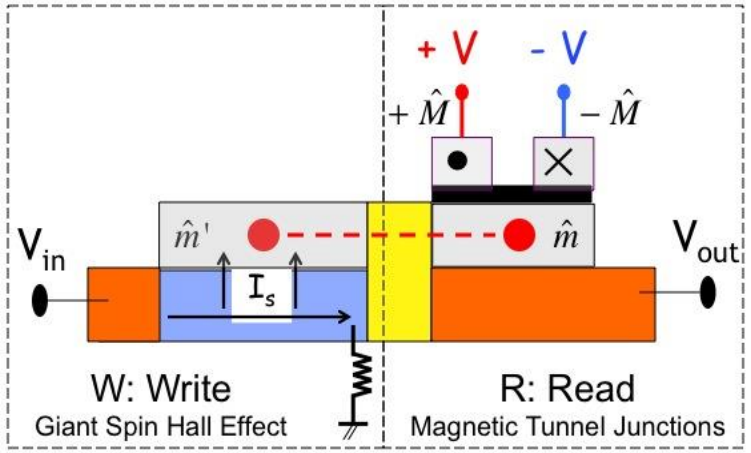
STT can switch magnetization of a free layer in a magnetic tunnel junction (MTJ) by switching current direction.

Berger, J. Appl. Phys. **55**, 1954 (1984)
Slonczewski, JMMM **159**, L1 (1996)
Berger, Phys. Rev. B **54**, 9533 (1996)

Charge-controlled Spin Logic

Datta, Salahuddin, and Behin-Aein, Appl. Phys. Lett. 101, 252411 (2012)

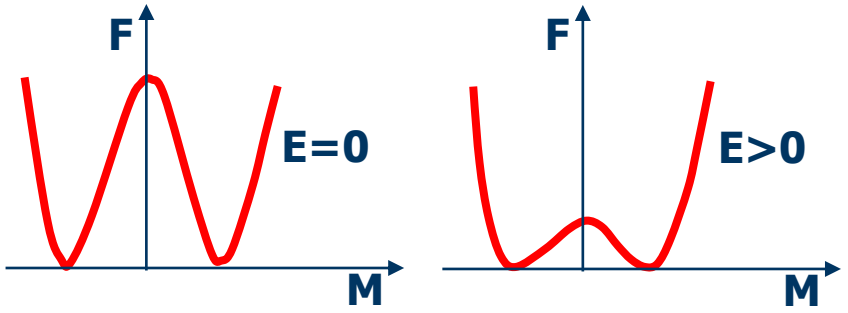
Spin switch



- Current from one device can switch others → *concatenating* logic
- Magnets retain logical state when power is off → *non-volatile* logic

Voltaged-switched (Magnetoelectric) Devices:

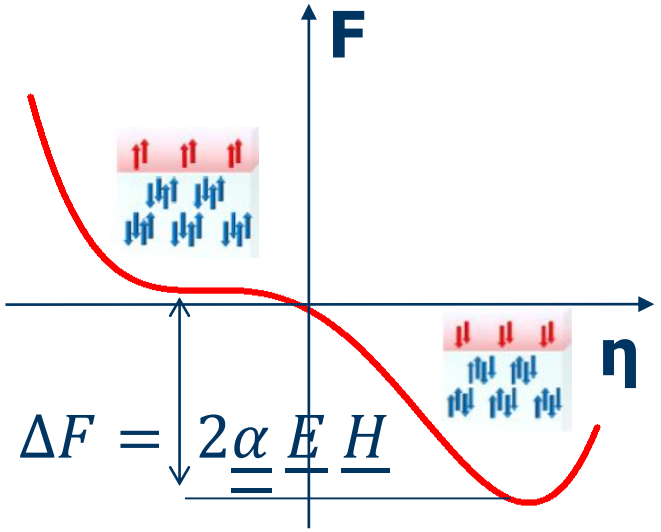
Two Mechanisms for Magnetization Reversal



Voltage Controlled Anisotropy

No thermodynamically preferred state, but precise timing of voltage pulses allows deterministic switching.

J.T. Heron *et al.*, Nature **516**, 370 – 373, (2014).



Voltage Controlled Exchange Bias

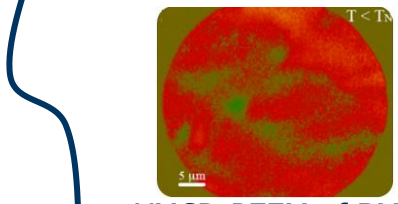
Applied voltage determines the thermodynamically preferred state.

X Hie *et al.*, Nature Materials **9**, 579–585 (2010).

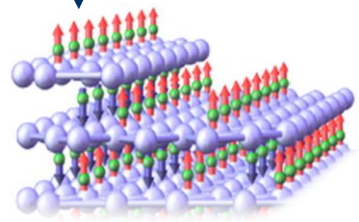
Magnetoelectric Antiferromagnets for Ultra-low Power Memory and Logic Device Applications

Goal: Voltage-switched ultra-low power MRAM
Approach: Reversal of free FM layer in perpendicular magnetic tunnel junction (p-MTJ) in the absence of electric current, based on voltage switching of the boundary magnetization in an antiferromagnetic thin film.

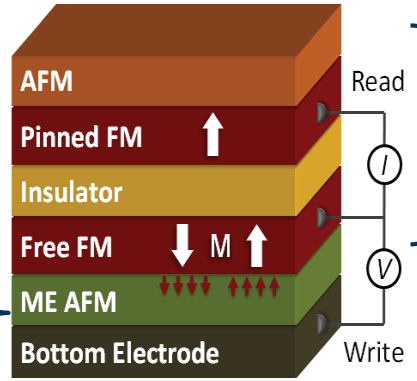
Boundary magnetization (BM) is a roughness insensitive generic property of antiferromagnetic materials.
K.D. Belashchenko, Phys. Rev. Lett. **105**, 147204 (2010)



XMCD-PEEM of BM



Magnetoelectric (ME) Cr_2O_3



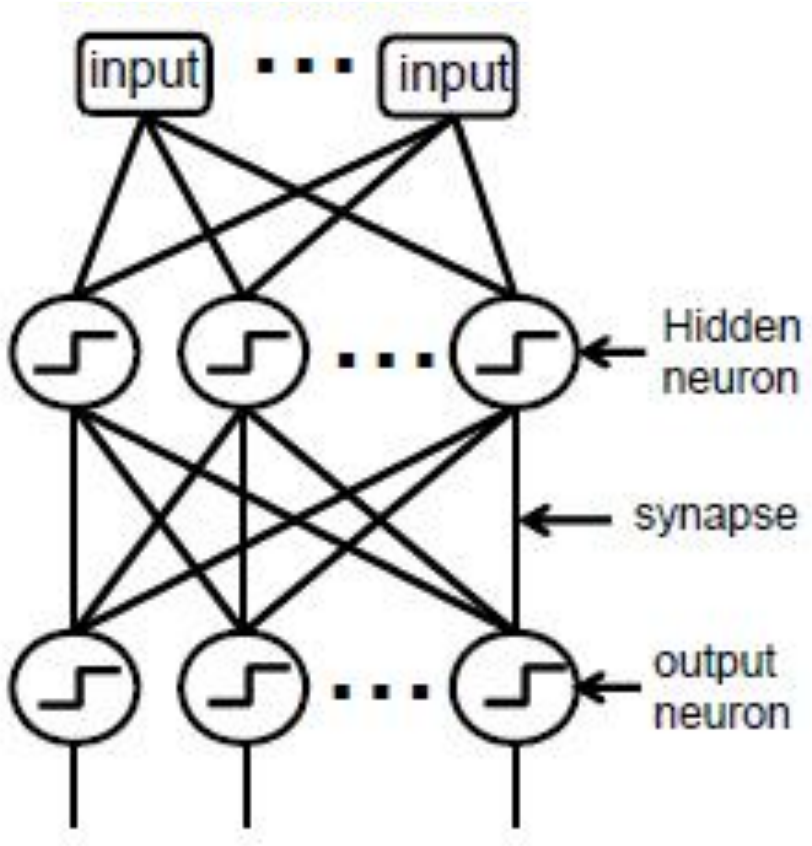
Read out of non-volatile memory state through tunnel magneto-resistance of p-MTJ or potentially through inverse ME effect

Magnetization orientation of FM layer is voltage - controlled through BM of ME antiferromagnet

An Assessment of Current Device Research

- While no clear winner has emerged, the rate of invention of new device concepts is increasing. It is therefore unlikely that we have already found the ultimate switch for digital computing.
- No truly new device will be a "drop in" replacement for the CMOS FET. Devices and circuits must be co-developed.
- Some devices may have characteristics that are particularly well suited to new and emerging architectures for computing.

As one example of a broad class increasingly important architectures, consider a Feed–forward Neural Network.



The computation in each node is simple.

Can it be done by a single device?

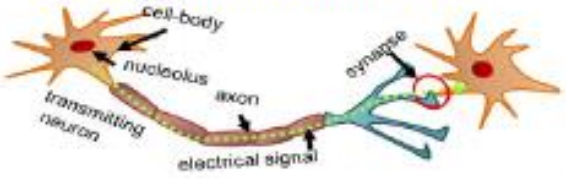
Spin-Neuron Based Feed-Forward Neural Network

Sharad, Fan, Roy et al. DAC 2013/ TNANO 2014/ JAP 1014

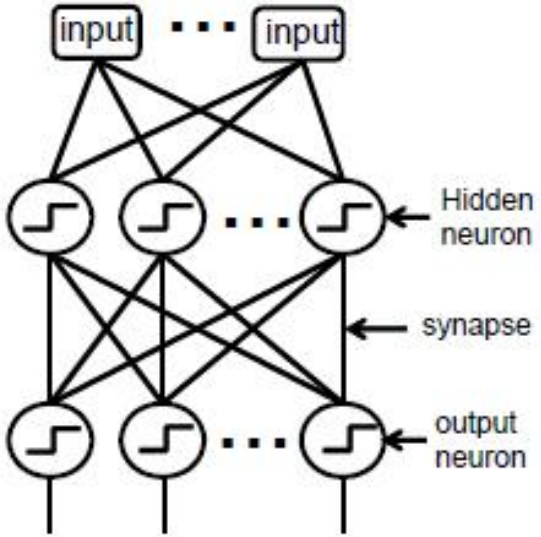
Spin-Neuron Based Feed-Forward Neural Network

Sharad, Fan, Roy et al. DAC 2013/ TNANO 2014/ JAP 1014

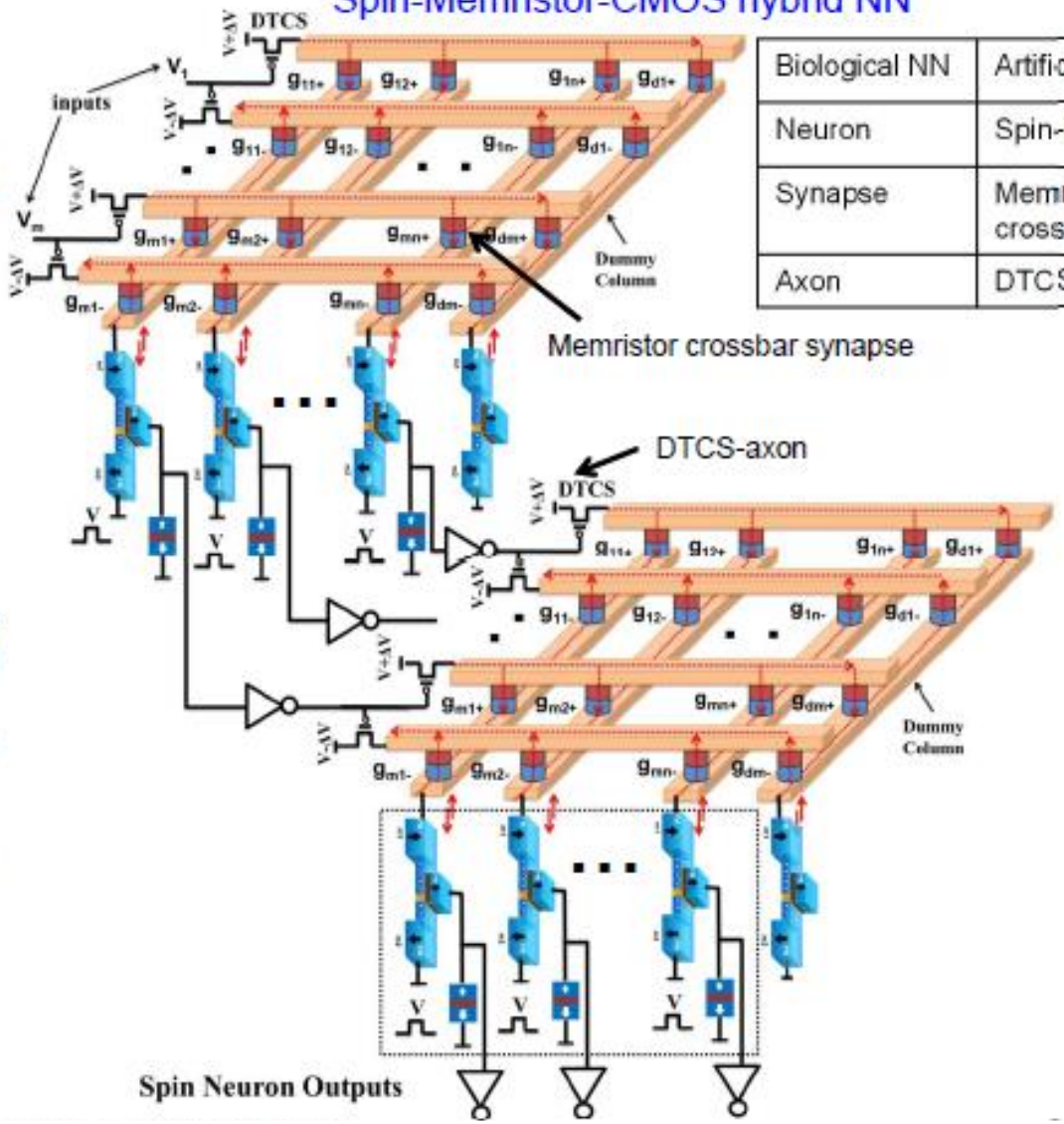
Biological neural network



Feed-forward NN



Spin-Memristor-CMOS hybrid NN



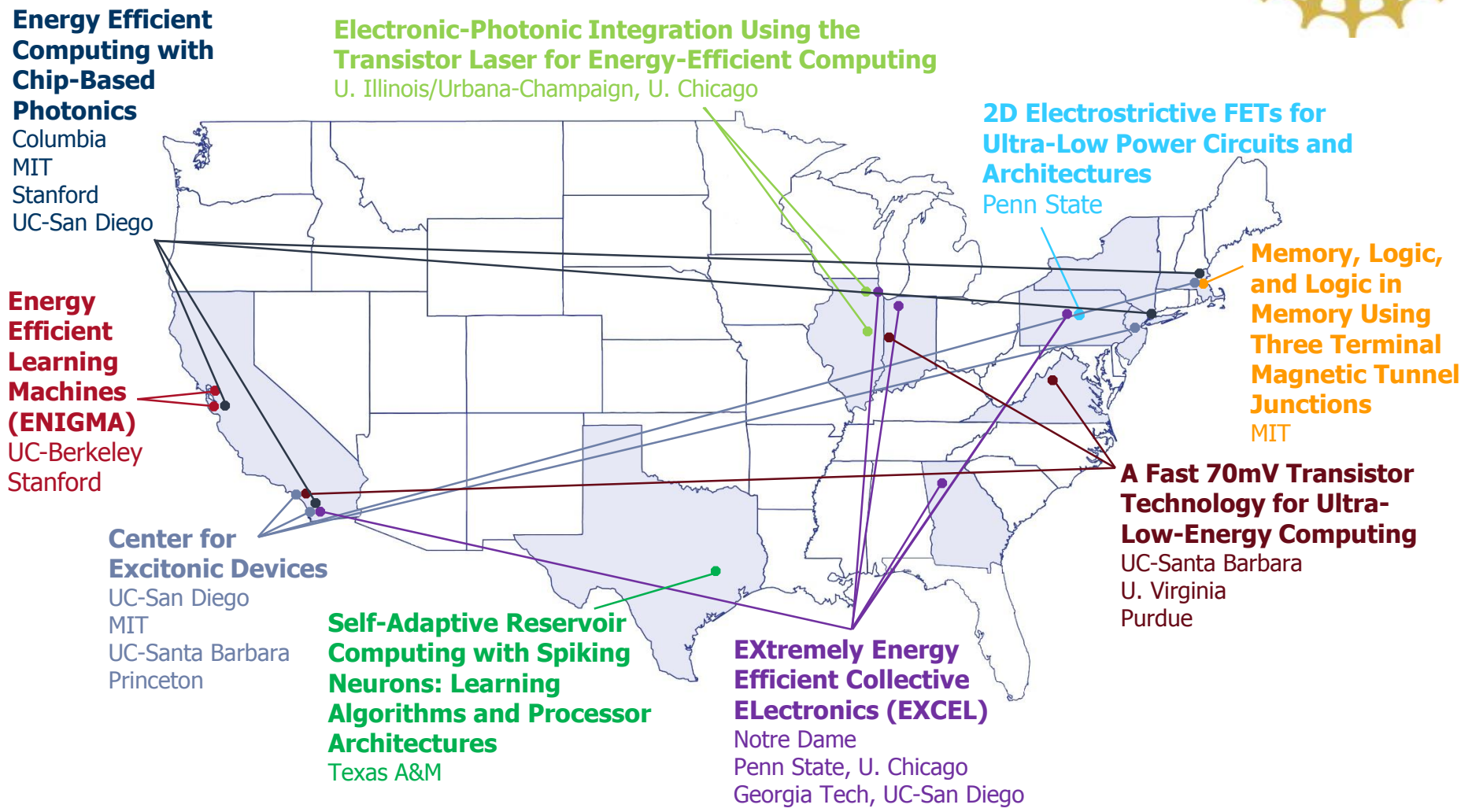
Biological NN	Artificial NN
Neuron	Spin-Neuron
Synapse	Memristor crossbar
Axon	DTCS

The Unexplored Research Landscape:

New Devices *and* New Architectures

E2CDA

Energy Efficient Computing: from Devices to Architectures
Funding 15 Universities in 10 States



Just Announced: E2CDA is Growing!

NSF17-531

Energy-Efficient Computing: from Devices to Architectures (E2CDA)
A Joint Initiative between NSF and SRC

https://www.nsf.gov/pubs/2017/nsf17531/nsf17531.htm?WT.mc_id=USNSF_25&WT.mc_ev=click

- Full proposals due March 07, 2017
- Directorate for Computer & Information Science & Engineering
  Division of Computing and Communication Foundations
- Directorate for Engineering
  Division of Electrical, Communications and Cyber Systems

Conclusion

Looking beyond conventional FETs
and the von-Neumann architecture,
there is a lot to explore!

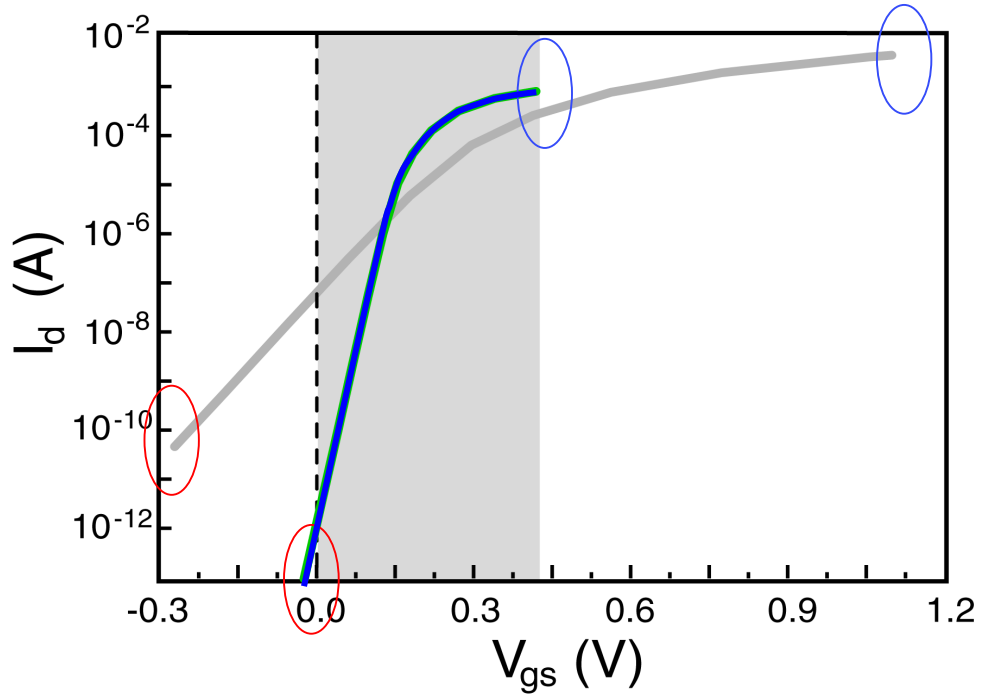
Thanks!

There are many potential paths to
truly low-power digital logic.

For now, let’s restrict ourselves to FET-like devices
that can operate at much less than 1 volt.

Low-voltage Current-switching Mechanisms and Some Exemplar Devices

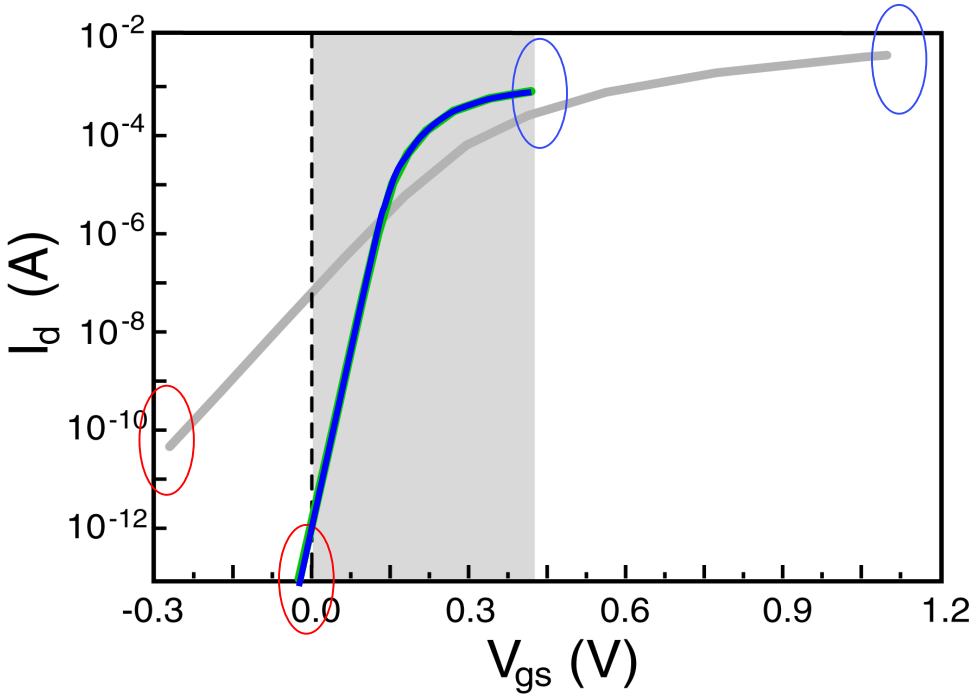
- **Energy Filtering**
  - Tunnel-FET
- **Internal Potential Step-up**
  - Ferroelectric-Gate FET
- **Internal Transduction**
  - Electromechanical Relay
  - Spin-FET
- **Gated Phase Transition**
  - Bi-layer Pseudo-spin FET (BiSFET)



BLUE: Discussed in Theis and Solomon, *Proc. of the IEEE*, Dec. 2010

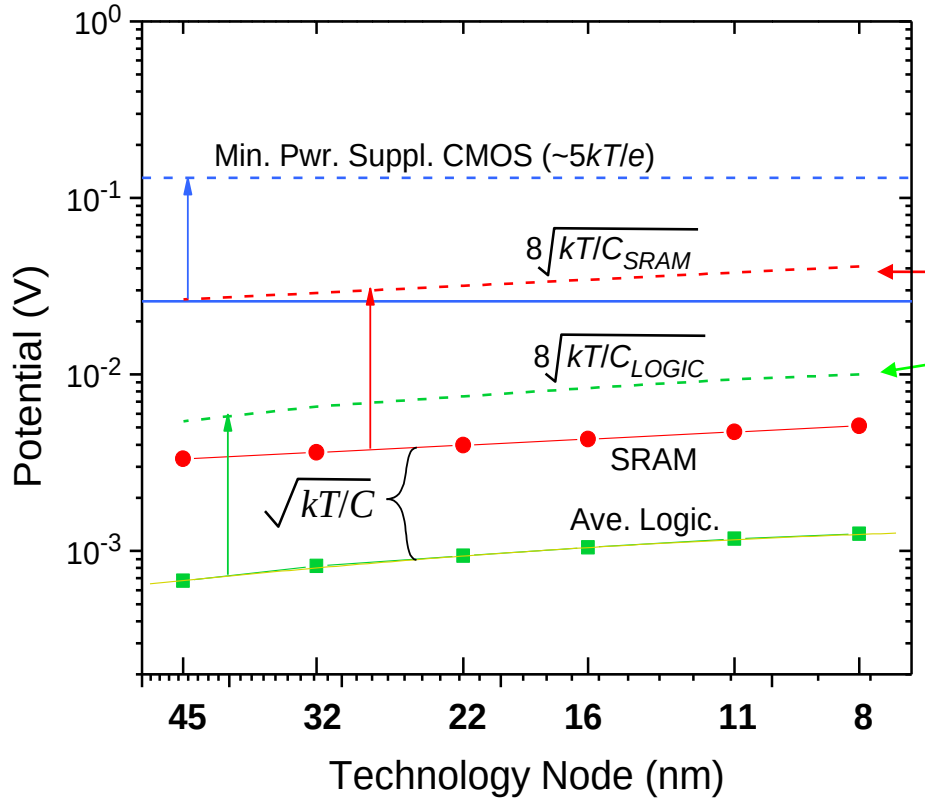
Low-voltage Current-switching Mechanisms and Some Exemplar Devices

- **Energy Filtering**
  - Tunnel-FET
  - Graphene p-n Junction Device
- **Internal Potential Step-up**
  - Ferroelectric-Gate FET
  - NEM FET
  - PiezoFET
- **Internal Transduction**
  - Electromechanical Relay
  - Spin-FET
  - PiezoElectronic Transistor (PET)
- **Gated Phase Transition**
  - Bi-layer Pseudo-spin FET (BiSFET)
  - Gated MIT, CDW transition, etc.



BLUE: Discussed in Theis and Solomon, *Proc. of the IEEE*, Dec. 2010
RED: Concepts proposed since 2010

A More Fundamental Limit:
Minimum Supply Voltage based on Voltage Noise Constraints



minimum 8σ Johnson-Nyquist noise criterion ($8\sqrt{kT/C}$) for
static memory
logic

Theis and Solomon, IEEE Proceedings **98**, pp. 2005-2014, Dec. 2010

Estimated average capacitance for logic includes both device and wiring capacitance, and for static memory, the internal capacitance of a 6-device cell.

Topics

- Post-CMOS Device Research – the Need and the Vast Opportunity
- Growing Research Investment
- Two Broad Classes of Emerging Devices
  - "Steep Slope" Devices (TFETs and More)
  - Nanomagnetic Devices (Spintronics)
- Conclusion: Devices *and* Architectures – the Unexplored Research Landscape