Novel Nanoelectronic Synaptic Memory Devices for Neuromorphic Computing

Alexander Jones[1], Tony Bailey[1], Andrew Rush[1], Sam Wenke[1], Thomas Schultz[1], Md. Sarim[2], Manish Kumar[2] and Dr. Rashmi Jha[1]

[1]Dept. of Electrical Engineering and Computing Systems, [2]Dept. Of Mechanical and Materials Engineering

University of Cincinnati, Cincinnati, Ohio, 45221; Rashmi.jha@uc.edu, Phone:513-556-1361

Introduction

The objective of this research is to develop nanoelectronic synaptic memory devices that can be used for implementing artificial cortical circuitries which can operate with the energy-efficiencies of a biological brain. A biological synaptic element can be strengthened or weakened on varying time scales which reconfigures the connection between neurons.

Challenges

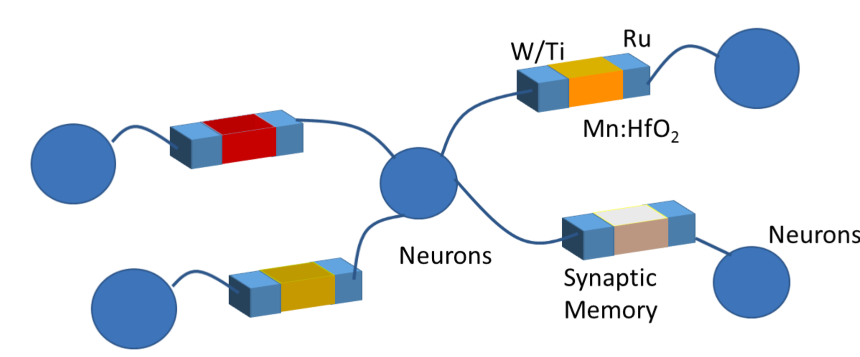
The current set of challenges lie ahead in the field of neuromorphic computing that our research group is working towards tackling. The challenges lay themselves out in a hierarchical format that penetrate into all levels of design.

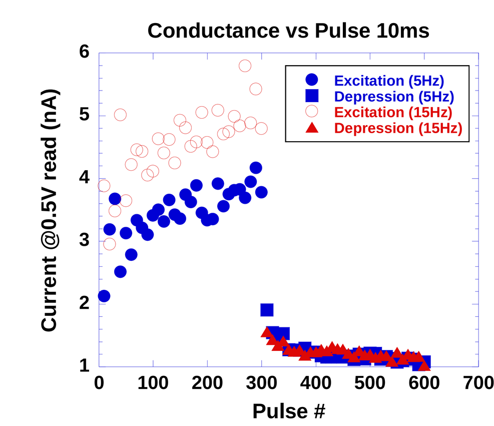
1. Material research must be conducted to find proper materials to fabricate nanoscale synapses and neurons that are reliable, durable, replicable, and scalable.
2. Scalable device design for both synapses and neurons must be researched in order to ensure the potential for high density architecture designs.
3. Neuromorphic architecture designs using these devices must not only be efficient in terms of space, but in other factors such as power.
4. The neuromorphic architecture must also have proper means to interface with other computer systems and devices such as external sensors.

Research Progress

Synaptic Memory Devices

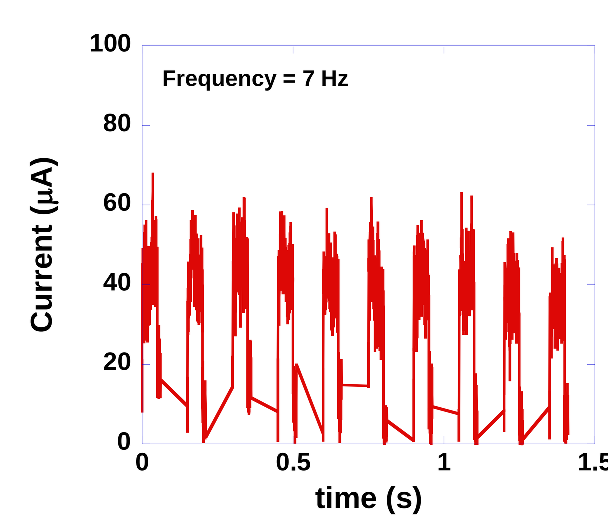
Doped transition metal oxide based devices were developed that showed reconfigurable multiple resistive states indicating potential for long-term potentiation and long-term depression using appropriate voltage pulses [1].

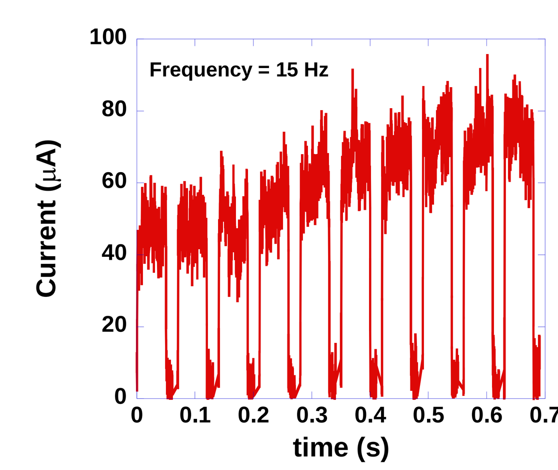




Short Term Plasticity

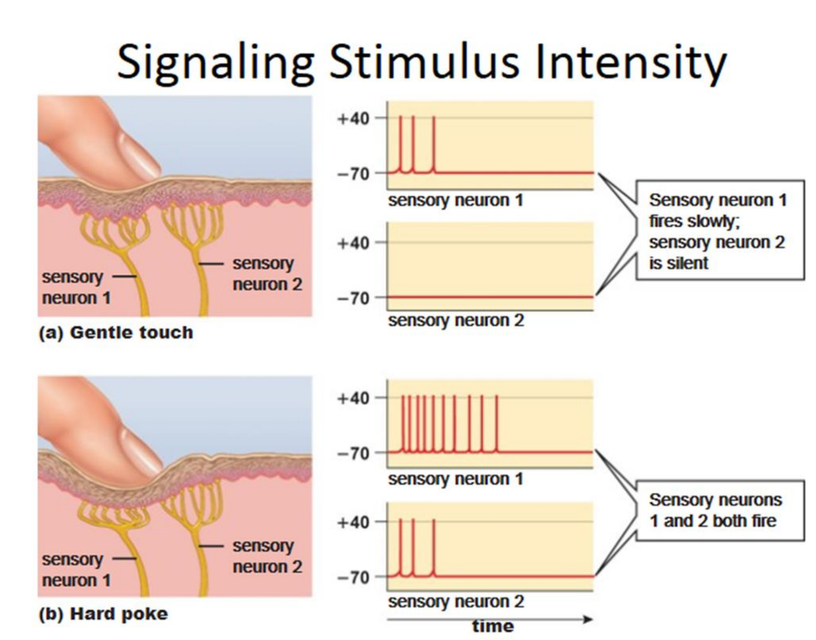
Short Term Plasticity (STP) of synapses is known to play a key role in decision-making and working memory formation in biological brains. STP was observed in nanoelectronic synapses [2].





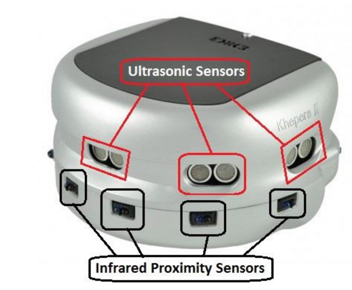
Neuronal Design

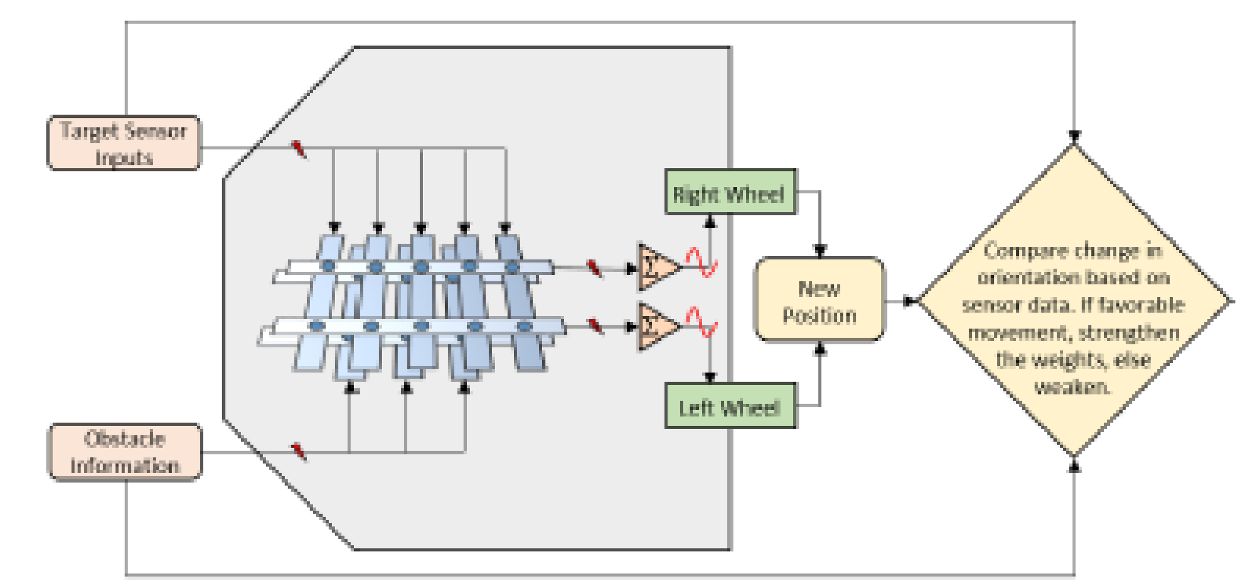
To process data from sensors in neuromorphic circuits, it is critical to develop sensory neurons that can convert sensor outputs into corresponding spike frequencies [3]. Our team is working on developing nanoscale neurons to mimic the functionality of sensory neurons.



Neuromorphic Architecture Design

Energy-efficient Neuromorphic architectures are being developed using nanoscale synapses and neurons. Appropriate learning algorithms are being investigated that are suitable for implementation on these hardware platforms. We are exploring applications of these architectures in obstacle avoidance and navigation of miniature mobile Robots [4].





Conclusions

- Nanoelectronic Synaptic Memory devices are developed using doped transition metal oxide.
- Both Long-term and short-term changes in synaptic conductance is observed.
- Application is demonstrated in navigation and obstacle-avoidance of mobile robots.

References

[1] Mandal et. al. Nat. Sci, Rep., 2014. [2] Sandal et. al. IEEE TED, 2013, [3] Kandel, 5th Edition McGraw-Hill, [4] Sarim et. al. IEEE NAECON, 2016.

Acknowledgements

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