# Hybrid Spintronics and Straintronics: A New Technology for Ultra-Low Energy **Computing and Signal Processing Beyond the Year 2020 (NEB: 1124714)** P.I.: Supriyo Bandyopadhyay

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--**⊟**-- 90 ps

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Stress (MPa)

¥ 350

300

250

- > Fast ramp rates and higher stress levels are conducive to successful switching.
- $\succ$  Sub-nanosecond switching delay is achievable. • Switching delay decreases with higher stresses and faster ramp rates.
- Energy dissipation of only 200 kT at room temperature with thermal mean switching delay 0.5 ns for 15 MPa stress and 60 ps ramp duration.
- $\rightarrow$  Application in energy-efficient non-volatile memory.

Roy puter , Rich		Stud D Virgi
	2-STATE STRAINTRONICS FO	OR LOG
	<ul> <li>Multiferroic nanomagnetic "wires": Bennett-clocking ~ 1 GHz with electrostatic potential of ~ few mV applied to the piezoelectric layer.</li> </ul>	1stMagnet 2nd Magnet Initial Ĵ ↓
	<ul> <li>All multiferroic nanomagnetic NAND gate with fan-in/fan-out: simulated using the Landau-Lifshitz-Gilbert (LLG)</li> </ul>	Magnet-1 switched ↓ ↓ ↑ and ↓ tie Apply Stress to Magnet 2, 3 ↓
g	<ul> <li>Clocking in multiferroics</li> <li>→3-5 orders of magnitude more energy efficient than other current method for rotating the magnetization direction through large angles</li> </ul>	Remove stress to Magnet 2
llus. (e.g.,	<ul> <li>✓ J. Atulasimha and S. Bandyopadhyay, Appl. Phys. Lett. 97, 173105, 201</li> <li>✓ M.Salehi Fashami, K.Roy, J.Atulasimha, S.Bandyopadhyay Nanotechnology 22 ,155201, 2011.</li> <li>✓ M Salehi Fashami, J.Atulasimha, S.Bandyopadhyay, Nanotechnology (under review), arXiv:1108.5758, 2011.</li> </ul>	
	MAGNETIZATION DYNAMICS: "W	IRES" &
	Magnetization dynamics in multiferroic nanomagnetic logic $\frac{\text{The Landau-Lifshitz-Gilbert (LLG) Equation}}{\frac{d\vec{M}(t)}{dt} = -\gamma \vec{M}(t) \times \vec{H}_{eff}(t) - \frac{\alpha \gamma}{M} \left[ \vec{M}(t) \times \left( \vec{M}(t) \times \vec{H}_{eff}(t) \right) \right] \qquad $	to energy of $U_i(t)$
on	$H_{eff}(t) = -\frac{1}{\mu_0 \Omega} \frac{1}{\partial M_i(t)} = -\frac{1}{\mu_0 \Omega} \frac{1}{\partial M$	$\overline{M_s\Omega} \nabla_{\vec{m}} U_i(t)$
0°	$U_{i}(t) = \sum_{\substack{j \neq i \\ i_{dipole-dipole}}} E_{dipole-dipole}^{i-j}(t) + \left(\frac{\mu_{0}}{2}\right) \left[M_{s}^{2}\Omega\right] \left(N_{d_{xxx}}\left[\sin\theta_{i}(t)\cos\phi_{i}(t)\right]^{2} + N_{d_{yyy}}\left[\sin\theta_{i}(t)\sin\phi(t)\right]^{2} + N_{d_{zzz}}\left[\cos\theta_{i}(t)\right]^{2} + N_{d_{zzz}}\left[\cos\theta_{i}(t)\sin\phi(t)\right]^{2} + N_{d_{zzz}}\left[\cos\theta_{i}(t)\right]^{2} + N_{d_{zzz}}\left[\cos\theta_{i}(t)\sin\phi(t)\right]^{2} + N_{d_{zzzz}}\left[\cos\theta_{i}(t)\sin\phi(t)\right]^{2} + N_{d_{zzzzz}}\left[\cos\theta_{i}(t)\sin\phi(t)\right]^{2} + N_{d_{zzzzzzzzzz}}\left[\cos\theta_{i}(t)\sin\phi(t)\cos\phi(t)\right]^{2} + N_{d_{zzzzzzzzzzzzzzzzzzzzzzzzzzzzzzzzzz$	me of Nanomagnet
ICS on due	ALL-MULTIFERROIC LOGIC WIR	ES AND
ps rants 60°)	R R R 430 R	pressive Stress o KT/bit @ 1GH
ess np rate	UNIVERSAL GATE: NAND LOGIC WITH FAN-OUT 1. Nanomagnets are clocked with electrostatic potential of ~50 mV applied to the piezoelectric layer generating 10 MPa	$\frac{1}{\sqrt{3/2}} R$
eld) I)	<ul> <li>stress in the magnetostrictive layers.</li> <li>2. Pipelined bit throughput rate of ~ 0.5 GHz is achievable with GATE sinusoidal four-phase clocking.</li> </ul>	$\mathbf{P} = \mathbf{A} \mathbf{R} \mathbf{R} \mathbf{R} \mathbf{R} \mathbf{R} \mathbf{R} \mathbf{R} R$
eks in	<ul> <li>3. Total Energy dissipation → ~ 500kT in the gate and ~1300 kT in the 12-magnet array.</li> </ul>	
ON	SIMULATION RESULTS: 2-STA	TE LO
	Bennett clocking in logic "wires" $\int \frac{e^{-52MP}}{\sqrt{99}} \int e^{-$	oic NAND gate

M Salehi Fashami, J.Atulasimha, S.Bandyopadhyay, Nanotechnology (under review), arXiv:1108.5758, 2011.

- The initial condition in all of cases are  $\phi_0 = \pm 85^0$ ,  $\theta_0 = 89.9^0$
- The NAND gate operation is completed in 2 ns with a latency of 4 ns.
- The total energy dissipation in the gate is respectively 3 and 5 orders of magnitude more energyefficient than complementary-metal-oxide-semiconductor-transistor (CMOS) based and spin-transfertorque-driven nanomagnet based NAND gates.

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### HC









on magnet 2 & 3. Iz in the wire.



GIC



- four stable magnetization directions.
- NOR logic: apply clock cycle, involving a sequence of stresses to the output nanomagnet, with an input nanomagnet on each side of it.
- Stress Sequence: Tension (T)  $\rightarrow$  Relaxation (R)  $\rightarrow$ Compression (C)  $\rightarrow$  Relaxation (R)



- The 4 stable magnetization states of the
- Noise can corrupt the image by perturbing
- Magnetization dynamics studied by solving

 $E_{total}(t) = E_{magnetocrystalline-anisotropy}(t) + E_{shape-anisotropy}(t)$  $\frac{d\mathbf{n}_{\mathbf{m}}(t)}{dt} - \alpha \left( \mathbf{n}_{\mathbf{m}}(t) \times \frac{d\mathbf{n}_{\mathbf{m}}(t)}{dt} \right) = \frac{-\gamma}{M_{s}\Omega} \mathbf{T}_{\mathbf{E}}(t)$  $\mathbf{T}_{\mathbf{E}}(t) = -\mathbf{n}_{\mathbf{m}} \times \nabla E_{total}(\theta(t), f(t))$ 





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