A Perspective in Nanoelectronics

Mark Lundstrom

Electrical and Computer Engineering
and
Network for Computational Nanotechnology
Birck Nanotechnology Center
Purdue University, West Lafayette, Indiana USA
Moore’s Law?

Minimum Feature Size

Year

~1995 - 2000
~1995 - 2001

Moore’s Law: what happened?

http://en.wikipedia.org/wiki/Moore's_law

G. Dan Hutchenson, “The First Nanochips,” Scientific American, April, 2004
Moore’s Law on a linear scale

transistors per cpu chip

Billions of transistors

Year

2010 - 2020

Moore’s Law?

How far below 8 nm can we go?
nanoscale MOSFETs: 2010

- Source (S)
- Gate (G)
- Drain (D)

- Silicon
- Gate oxide (EOT ~ 1.1 nm)
- Channel ~ 22 nm

- Gate electrode

- Source
- Drain

- SiO₂
physics of transistors

2007 N-MOSFET

Electron energy vs. position

(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

limits of transistors

from M. Luisier, ETH Zurich / Purdue
limits of transistors (ii)


\[
E_S \bigg|_{\text{min}} = \ln(2) k_B T
\]

\[
L_{\text{min}} \approx \hbar \sqrt{\frac{2 m E_S}{E_S'}}
\]

\[
\tau_{\text{min}} \approx \hbar / E_S'
\]

\[
(\Delta p \Delta x = \hbar)
\]

\[
(\Delta E \Delta t = \hbar)
\]
Moore’s law forever?

When Gordon Moore predicted in 1965 that the number of transistors per integrated circuit chip would continue to double in each technology generation, there were just 50 transistors on a chip. Today, transistor counts—a measure of the capability of an electronic system—exceed a few hundred million for logic chips and even more for memory chips. How long can Moore’s law continue?

The semiconductor industry follows Moore’s law by shrinking transistor dimensions. But transistors cannot be scaled down infinitely. A few years ago, as critical dimensions approached 100 nm, a number of formidable challenges arose (1). It seemed that progress would slow, but during the past few years, device scaling has accelerated, as evidenced by several talks at the recent International Electron Devices Meeting (IEDM) (2).

Today’s electronic devices are based on the metal oxide semiconductor field-effect transistor (MOSFET), which consists of source and drain electrodes, through which current can flow, and a gate electrode, which controls the current through the other two (see the figure). MOSFETs operate on a simple principle: When the gate voltage is low, an energy barrier prevents electrons from flowing from source to drain, whereas a high gate voltage lowers the energy barrier, allowing current to flow (see the figure). The gate electrode is separated from the silicon channel by a thin insulating layer to prevent the flow of gate current.

To comply with Moore’s law, the transistor designer must shrink the distance between source and drain by a factor in each technology generation. This has been accomplished by a factor of 2, thereby doubling the number of transistors per chip. Remarkable advances in subwavelength lithography allow current-generation technologies with gate lengths of 65 nm to be manufactured. Economic considerations have not yet slowed progress, and state-of-the-art technology still operates far below the fundamental limits imposed by thermodynamics and quantum mechanics (3).

serious transistor design issues arise from materials limitations and transistor physics.

For digital applications, a transistor switch must, first, deliver a large on-current that rapidly charges and discharges the capacitance of the wires connecting it to other transistors in the circuit. The switching power is proportional to the operating frequency and to the square of the power supply voltage. Transistor scaling increases the number of gates on a chip and their operating frequency. To limit power dissipation and prevent the chip from overheating, the power supply voltage must therefore decrease in each technology generation, while maintaining the on-current.

Second, a transistor switch should conduct very little current when off. However, as the distance between the source and drain shrinks, it becomes increasingly difficult to turn a MOSFET off. Because off-currents increase exponentially with device scaling, the off-state power consumption is no longer negligible.

Third, transistors should switch on

"Moore’s Law is about lowering cost per function…progress continues at a breathtaking pace, but transistor scaling is approaching limit. When that limit is reached, things must change, but that does not mean that Moore’s Law has to end.”
21st century electronics?

molecular electronics

carbon nanotube electronics

flexible electronics

spin torque devices

nanowire PV

nanowire bio-sensors

nanowire thermoelectrics

CoFe (2.5)

Ru (0.85)

CoFeB (3)

MgO (0.85)

CoFeB (3)

HfO$_2$

10 nm SiO$_2$

p$^{++}$ Si

Al Gate

nanonets

$\text{L}_W$ $\text{L}_C$

thermoelectrics
atomistic / quantum effects in CNTFETs


electronics and biology/medicine

In the future ..
Nanodots ?

Recently ...
Si-NW/CNT

Historically ...
ChemFET/IsFET

M.A. Alam: Purdue University
NW sensors and the geometry of diffusion

\[ D_F = 2 \]

\[ D_F = 1 \]

M.A. Alam, “Geometry of Diffusion and the Performance Limits of Nanobiosensors,” www.nanoHUB.org

\[ N(t) = \rho_0 \times R \times A \]

\[ N(t) : \rho_0 \sqrt{Dt} \]

\[ N(t) = \rho_0 \times \pi R^2 \times L \]

\[ N(t) : \rho_0 Dt \]
$G = n_s q \mu_{\text{eff}} \frac{W_C}{L_C}$

$1 < D_F < 2$

John Rogers group, Univ. of Illinois
Ashraf Alam group, Purdue University

$G \sim \frac{1}{L_C}$

$G \sim \frac{1}{L_C^2}$
energy

modern solar cell

Pearson, 1954

http://www.nrel.gov/learning/re_solar.html
(1) Organic solar cells with phase segregated donor/acceptor regions.

(2) Performance is controlled by the nanostructure.

(3) A new conceptual and computational approach to problems of this class is being pioneered by M.A. Alam (Purdue). IEDM 2009, IRPS 2010
thermoelectric devices

\[ ZT = \frac{S^2 \sigma T}{K_e + K_L} \]

Bi₂Te₃ and alloys with Sb, Se

randomness is the rule

1997 MOSFET (Texas Instruments)

Random Dopant Fluctuations

after Takahiro Shinada, et al., *Nature*, 437, 1128, 2005
challenges

1) **Learning** to build, characterize, simulate, design, and understand a wide variety of new devices at the nanoscale.

2) Identifying the *right applications* for these novel technologies.
"SEEC was a triumph of engineering science, with a substantial, lasting impact… The approaches are still used in EE education throughout the world…"

re-thinking electronic devices

“Trying to explain things rigorously, but simply often requires new organizing principles and approaches.”

Paul Penfield
class notes on “Information”

“Electronics from the Bottom Up”
Taking the understanding that is emerging from research on unconventional nanoelectronics, and re-thinking the field of electronic devices from small to large.
Example: Seebeck coefficient

\[ \Delta V = S \Delta T \]


Graphene

source: CNTBands 2.0 on nanoHUB.org

\[ g_V = 2 \]

\[ E(k) = \pm \hbar \nu_F k \]
NCN / nanoHUB.org

user community.....

students

professionals

faculty

HUBzero IT platform

user and site support, SW development, service development, content development, assessment...

research community.....

faculty

research groups

research centers

technology for:
-dissemination
-collaboration
-online simulation / data

Google: “Electronics from the Bottom Up”
1) Nanotechnology has captured the imagination of young people and fostered collaborations across disciplines.

2) CMOS technology continues to evolve, the NNI played an important role - the consequences of incremental advances will be truly revolutionary.

3) Nanotechnology is developing new understanding, tools for simulation, metrology and fabrication, and building blocks that will support technology evolution and ultimately re-shape technology.

4) In the next decade, we need on turning nanoscience into nanotechnology. 1) Find the right applications and 2) Understand the technology landscape.