Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

nanoelectronics RESEARCH INITIATIVE

SRC Nanoelectronics Research Initiative

Overview for NSF Grantees Meeting
December, 2008

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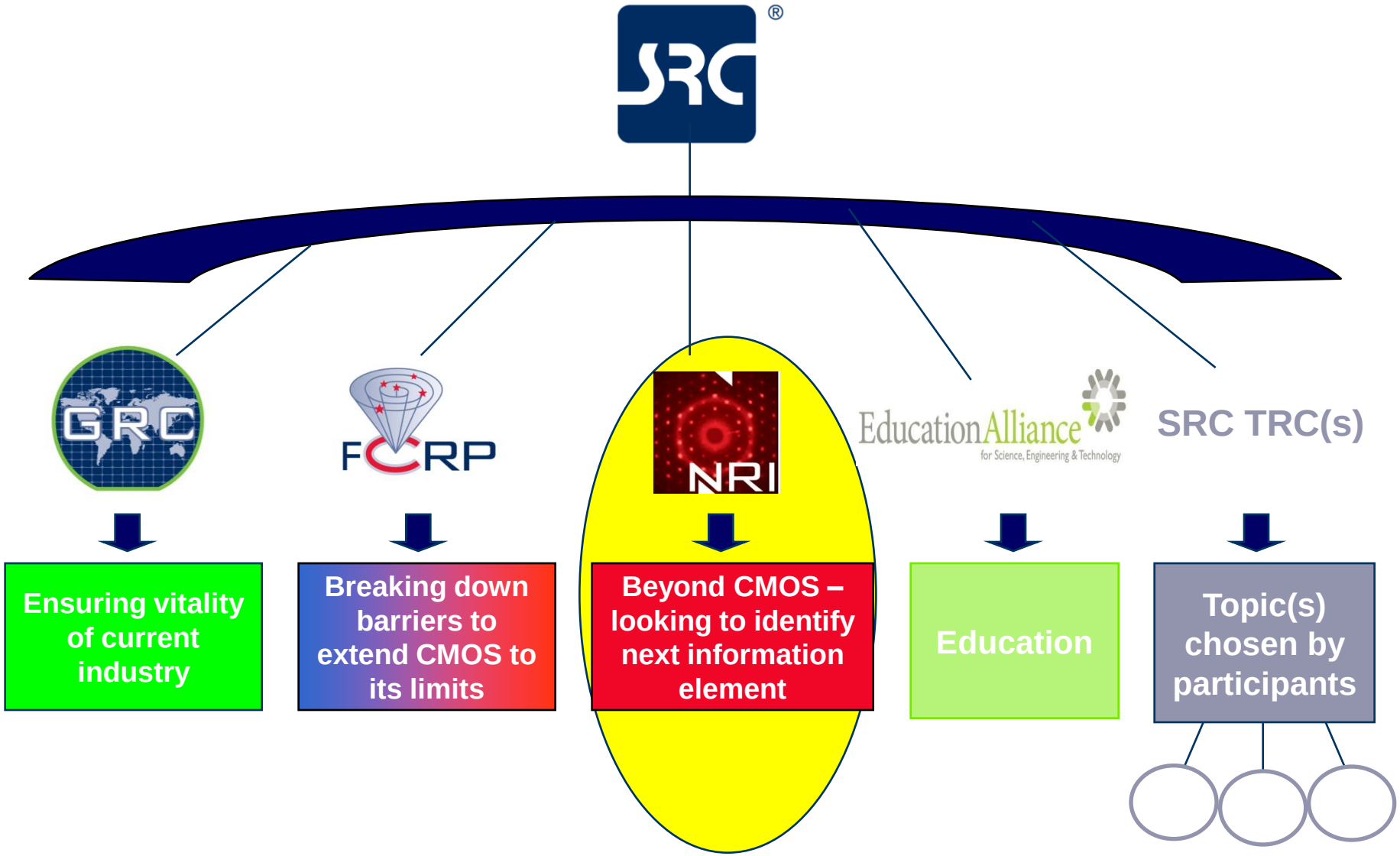
SRC Brands: A Family of Distinct but Related Program Entities



Nanoelectronics Research Initiative Milestones

- 2001-2004: Defining Research Needs
  - ITRS-Emerging Research Device Technical Working Group
  - NSF-SRC Ind-Academia-Govt "Silicon Nanoelectronics and Beyond" Workshops
  - SIA Technology Strategy Committee workshops
  - ➢ *Defined 13 Research Vectors for finding the "next switch"*
  - ➢ *March, 2004: SIA Board passes resolution for formation of NRI*

- March 2005: Six Companies sign NRI Participation Agreement

- Sep 2005: First NRI and NRI-NSF Solicitations released
- Jan 2006: Research Programs started

- Sep 2007: NIST joins NRI
  - Program expanded and extended through 2010

- NRI partnership model highlighted in a sidebar in the National Nanotechnology Initiative (NNI) Strategic Plan (NNCO, 1/08)

NRI Mission Statement

- **NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.**
  - These devices should **show significant advantage over ultimate FETs** in power, performance, density, and/or cost to enable the semiconductor industry to **extend the historical cost and performance trends** for information technology.
  - To meet these goals, NRI pursues **five research vectors**, focused on discovering and demonstrating new devices and circuit elements for doing computation.
  - Finally, it is desirable that these technologies be **capable of integrating with CMOS**, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

Beyond CMOS Logic: What are we looking for?

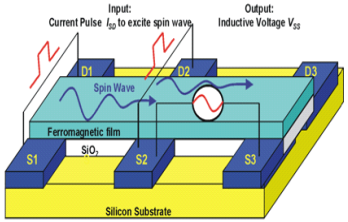
- **Required characteristics:**
  - **Scalability**
  - **Performance**
  - **Energy efficiency**
  - **Gain**
  - **Operational reliability**
  - **Room temp. operation**
- **Preferred approach:**
  - **CMOS process compatibility**
  - **CMOS architectural compatibility**

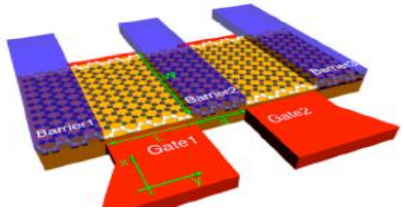
Alternative state variables

- Spin–
  electron, nuclear, photon
- Phase
- Quantum state
- Magnetic flux quanta
- Mechanical deformation
- Dipole orientation
- Molecular state

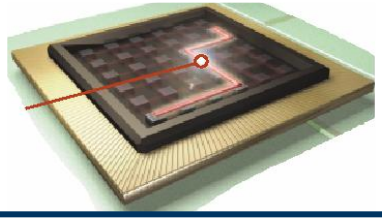
NRI Primary Research Vectors

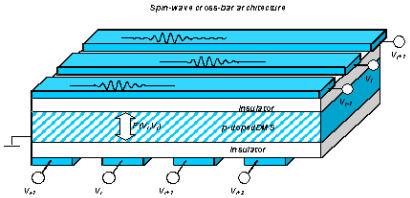
- **NEW DEVICE**
  Device with alternative state vector



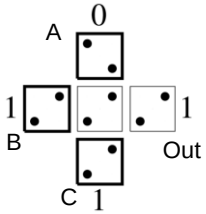


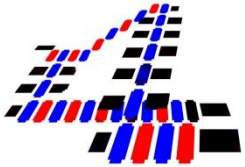
- **NEW WAYS TO CONNECT DEVICES**
  Non-charge data transfer



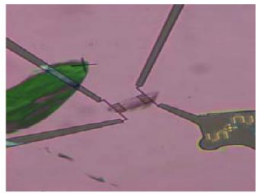


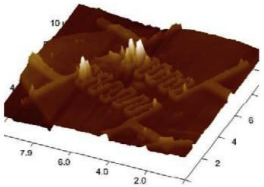
- **NEW METHODS FOR COMPUTATION**
  Non-equilibrium systems



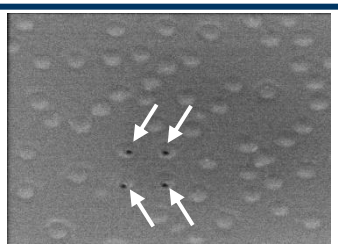


- **NEW METHODS TO MANAGE HEAT**
  Nanoscale phonon engineering





- **NEW METHODS OF FABRICATION**
  Directed self-assembly devices



NRI Centers

- Leveraging industry, university, and both state & fed government funds, and driving university nanoelectronics infrastructure

WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Iowa, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics Theme 4: Spin Metrology	Task I: Novel state-variable devices Task II: Fabrication & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap Task VI: Metrology	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Nanoscale thermal management Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Theme 1: Graphene device: Thermal, Tunnel, and Spin Theme 2: Interband Tunnel Devices Theme 3: Non-equilibrium Systems Model / Meas. Theme 4: Nanoarchitecture

NSF NSEC/MRSEC Nanoelectronics Areas*

3 Primary focus
2 Secondary focus
1 Very little or no focus

Question number		1	2	3	4	5
Institution		Alternative State variables	Non equilibrium devices	Novel information transfer	phonon engineering	self assembly
NSEC Centers						
Electronic Transport in Molecular Nanostructures, NSEC	Columbia University	1	2	1	2	2
Nanoscale Systems and their Device Applications, NSEC	Harvard University	3	3	3	3	3
Integrated Nanopatterning and Detection, NSEC	Northwestern University	1	2	1	1	3
Center for High Rate Nanomanufacturing	Northeastern University	2	1	1	1	3
Stanford Center for Probing the Nanoscale	Stanford	2	1	1	1	1
Center for Nanoscale Electrical-Mechanical Manuffacturing Systems	UIUC	1	1	1	2	2
Nanoscience in Biological and Environmental Engineering (CBEN)	Rice University	1	1	1	1	1
MRSEC Centers						
Biomaterial microstructures	UCSB	2	1	1	1	3
Grain boundaries, metals / ceramics; simulations	CMU	1	1	1	1	1
Princeton Center for Complex Materials	Princeton	3	1	1	1	3
Center for Nanostructered Materials	Cornell	2	1	1	1	2
Nanomagnetisms -fundamental interactions and applications	U of Nebraska	2	1	1	1	2
Nanoscopic design, quantum dots, surfaces	U ov Virginia	2	1	1	1	3
Transport in nanostructured magnetic materials	U of Alabama	3	3	1	1	2
Molecular motors	Penn State University	1	1	2	1	3
The Center for the Science and Engineering of Materials (CSEM),	California Institute of Technology	2	2	3	2	1
Laboratory for Research on the Structure of Matter	U of Pennsylvania	1	1	1	1	1
The Center for Materials Science and Engineering (CMSE)	MIT	2	1	1	1	2
Directed Assembly of Nanostructures, NSEC	Rensselaer Polytech Inst	2	1	1	2	3
Structural integrated films containing nanoparticles	Columbia University	1	1	1	1	3

*NSF-funded centers, capabilities self-assessed by Center directors

NSF-NRI Projects

18 Projects at 12 Centers

Columbia NSEC	*2006: Non-equilibrium Quantum Coherent Devices in 1-D materials* *2008: Novel Device Arch. based on Quantum Transport Phenomena in Graphene*
UCSB MRSEC (+Stanford, U Mass)	*2006: Development of Next Generation Devices using Nanolithography*
Harvard NSEC	*2006: Ultrasmall Nanowire and Oxide Switches* *2008: Tunable Ultra-fast Conductance Switching through External Fields*
U. Arkansas/U. Oklahoma MRSEC	*2006: Nanoferroelectric Random Access Memory*
Purdue NCN	*2006, 2007: Exploratory Theory, Modeling, and Simulation for the NRI* *2008: Experimental Realization of Low-power Transistors with Negative Capacitors*
UVA MRSEC (+Notre Dame, UCSB)	*2006: Directed Assembly of Epi Semiconductor Nanostructures for Novel Logic Switches; 2007: Coherent Spin Dynamics in Single Ion-doped Semiconductors: Towards a Coherent or Quantum Spin Switch*
U. Nebraska MRSEC	*2007: Multiferroic Interfaces: New Paradigms for Functional Switching*
Yale MRSEC	*2007: Design and Fab of Magnetic-based Devices with Complex Oxide Materials*
Maryland MRSEC	*2007: Pseudospintronics (+UT-Austin)* *2008: Controlling the Electronic Properties of Graphene*
Cornell NSEC	*2007: Controlled Orbital Hybridization in the CNT Quantum-Modulated Transistor*
Stanford NSEC (+UI-UC)	*2008: Ultra-Low Power Pseudospintronic Switching in Bilayer Graphene at Room T*
Caltech MRSEC	*2008: Graphene Atomic Switches for Ultracompact Logic Devices and NV Memory*

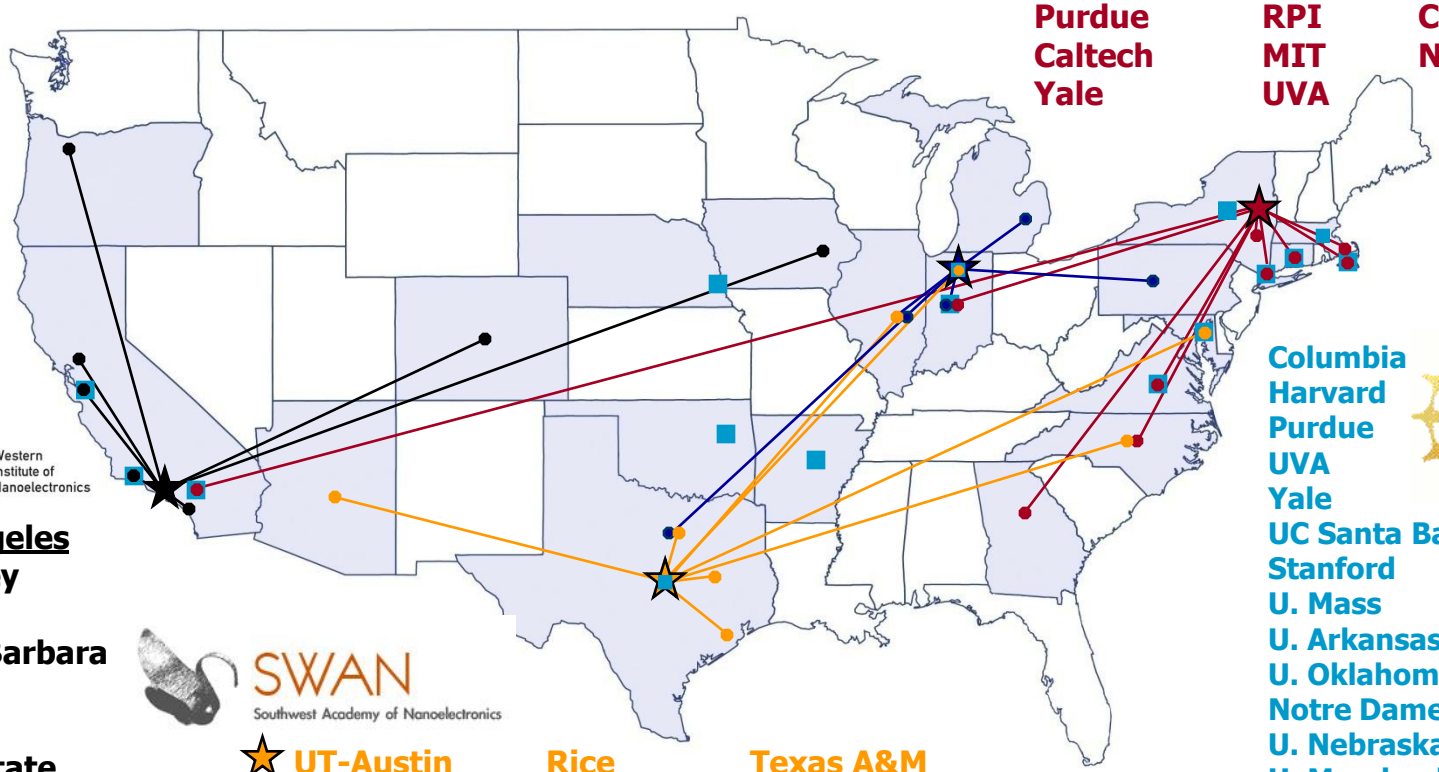
NRI Funded Universities

Nanoelectronics • Architectures
MIND
MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

★ **Notre Dame**
Illinois-UC
Michigan
Purdue
Penn State
UT-Dallas

INDEX
INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

★ **SUNY-Albany**
Purdue
Caltech
Yale
GIT
RPI
MIT
UVA
Harvard
Columbia
NCSU



WIN Western Institute of Nanoelectronics

★ **UC Los Angeles**
UC Berkeley
UC Irvine
UC Santa Barbara
Stanford
U Denver
Portland State
U Iowa

SWAN
Southwest Academy of Nanoelectronics

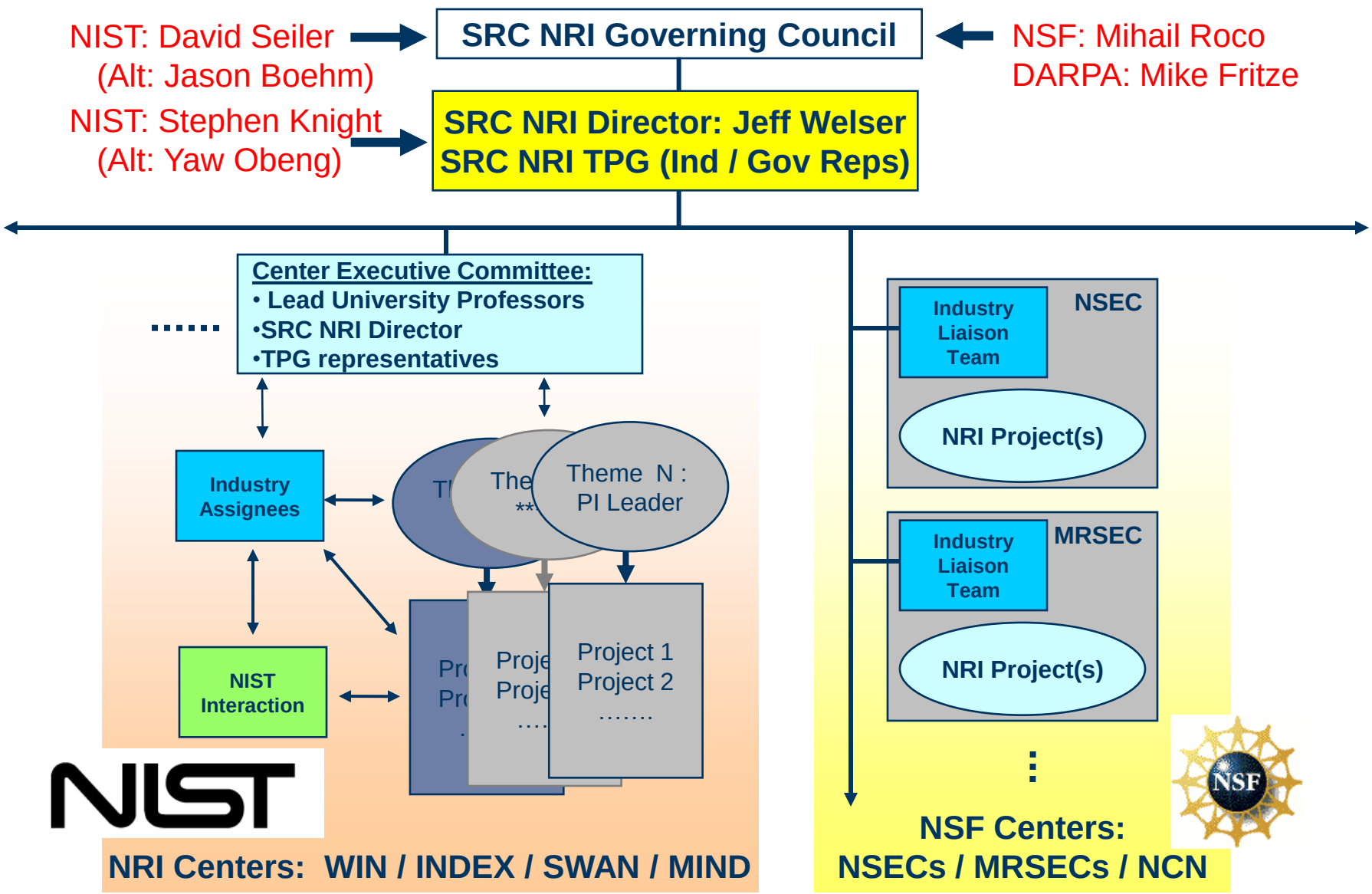
★ **UT-Austin**
UT-Dallas
U. Maryland
Rice
ASU
NCSU
Texas A&M
Notre Dame
Illinois UC

NSF

Columbia
Harvard
Purdue
UVA
Yale
UC Santa Barbara
Stanford
U. Mass
U. Arkansas
U. Oklahoma
Notre Dame
U. Nebraska/Lincoln
U. Maryland
Cornell
UT Austin
Caltech

Over 30 Universities in 20 States

SRC NRI Management Structure



NRI-NSF Joint Engagement

- NRI industry liaison team set up for each NSF center
  - Interact with PIs on NRI projects, learn about the work and give industry perspective
  - Broad discussions on other projects of mutual interest in the NSF center encouraged – including informing the rest of the center about the NRI program
- Visits each center at least once annually
  - Combine with any other NSF or external reviews for center, when appropriate
  - Encourage setting up quarterly telecons to enable on-going interaction
- PIs present at the NRI annual review Dec. 1-2, 2008 in Arlington, VA
  - Combined with NSF Annual Grantees' Conference Dec. 3-5
  - Includes all NSF-NRI center projects, as well as the main NRI centers

Feedback from 2008 Center Reviews

- Much better focus of work in all centers around specific device ideas, working across PIs and universities
  - **WIN**: Continues spin focus, with particular multi-PI projects on spin-wave devices and multi-ferroics
  - **INDEX**: Created 4 cross-university Centers of Competency and Innovation (CCIs) around device areas:
    - Excitronic, QD Spin, Magnetic, and Graphene Devices
  - **SWAN**: Expanded focus on Graphene, from theory to devices to materials fabrication, including a new pseudospintronic device concept. Expanded metrology program, directly linked to the device work
  - **MIND**: Work just starting, but focus will be on tunneling and thermal transport for creating non-equilibrium architectures. Also leading cross-center device/architecture benchmarking efforts.

- Comment from industry sponsor at reviews:
  - "The NRI experiment is working. For understanding graphene, for example, the NRI team is probably the best in the world. We learned more about graphene for applications in the last 2 years than we would normally learn in 5 or more years due to focus in NRI on science for devices."

NRI Technical Directions

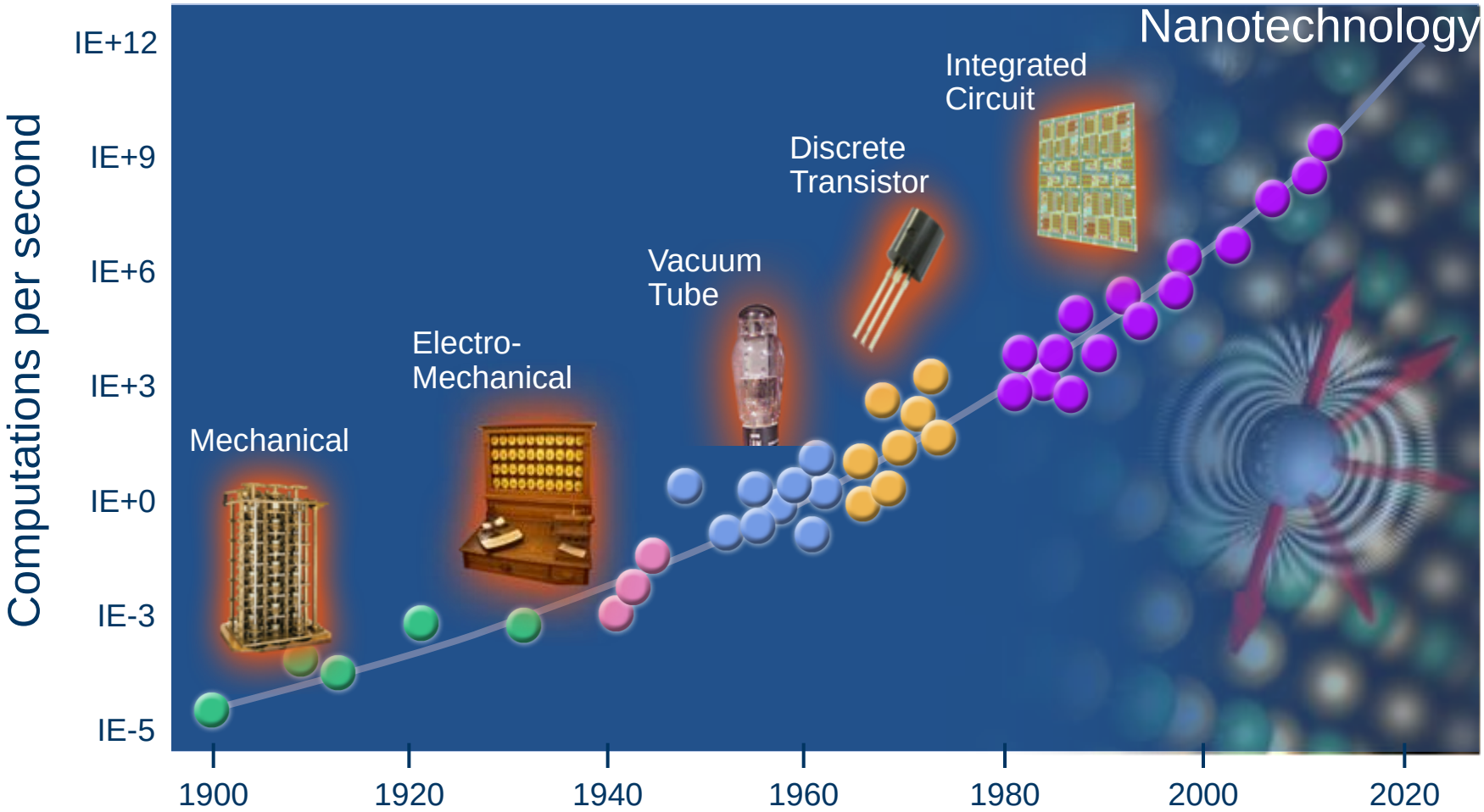
- NRI: A *goal-oriented*, *basic* research program to find the next switch
  - Centers continue to work on many phenomena ("thousand flowers bloom")
  - Success in integrating these more closely around device ideas in 2008

- Specific areas of focus for 2009:
  - Room temperature demonstrations of all phenomena
    - Plan to show RT results next year, or a "roadmap" in simulation to reach RT
  - Accelerate work to demonstrate theory – on simplified structures if needed
    - Theorists need to provide insight on how to verify effects in "realistic" structures
  - Increase focus on logic gate / computational system potential for devices
    - How to connect the devices, how to do logic, how to scale functional density
    - Started a weekly meeting on architecture benchmarking – planning a NSF/NRI workshop in 3Q09

- Increased emphasis on understanding computation device / system potential for NRI projects – Key questions:
  - Does it offer the prospect of operation / energy storage lower than CMOS?
  - Does it offer the prospect of non-equilibrium (e.g. ballistic) operation?
  - Does it offer the prospect of energy recovery?

NRI Goal: Continue the Curve . . .

$1000 Buys:



Source: Kurzweil 1999 – Moravec 1998

Questions? More Information?

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NSF 09-016: NSF-NRI Graduate Student and Postdoctoral Fellow Supplements to NSF Centers in Nanoelectronics (2009-2011)
http://www.nsf.gov/publications/pub_summ.jsp?ods_key=nsf09016
Deadline: February 20, 2009 → Contact NRI at least one month prior

Backups

Semiconductor Research Corporation: Collaboratively Sponsored University Research

- The Semiconductor Industry Association (SIA) members have recognized that collaboration among industry, government and academia is the most efficient means of advancing university research capabilities

- Strong university research is critical to maintain technology innovation
  - Research in new concepts, breakthrough ideas and solutions to problems for which no currently known solutions exist
  - Development of talent pool of scientists and engineers

- Semiconductor Research Corporation (SRC) has been established to facilitate collaboratively sponsored university research
  - Manages full spectrum of research related to CMOS and beyond technology

- Awarded the 2005 National Medal of Technology
  - "For building the world's largest and most successful university research force to support the … semiconductor industry …"