Emerging Nanoelectronic Devices

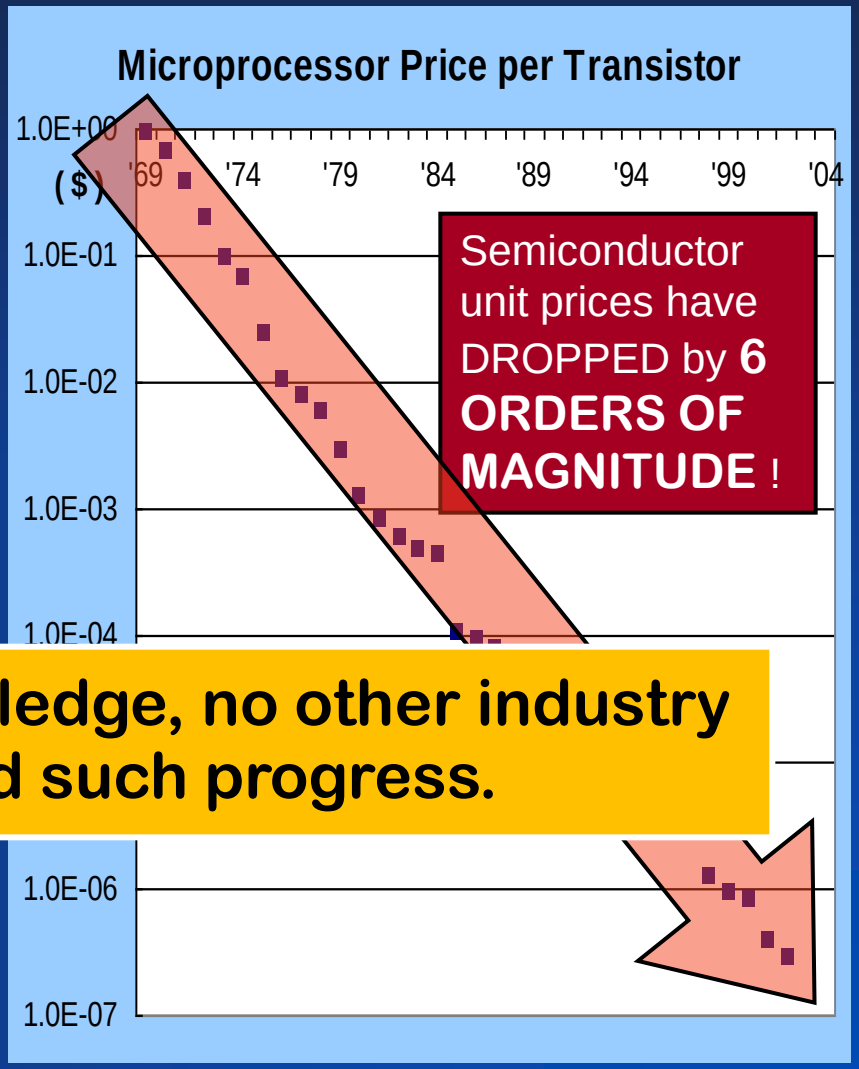
Ralph Cavin
Semiconductor Research Corp.

Historic Perspective

Over the past 35 years, prices for almost everything have CLIMBED by 5 -10 x.

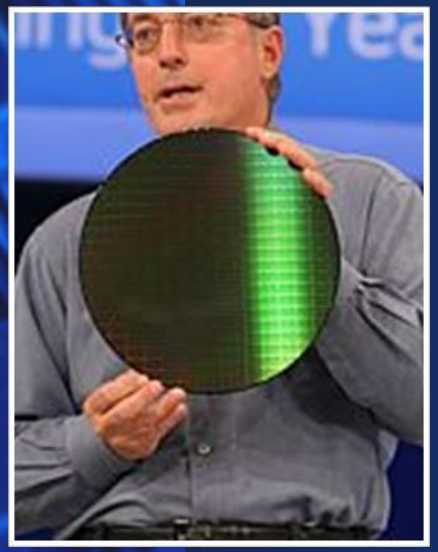
	1970	2008
Avg. Income	$9,300	$36,000
New House	$23,400	$215,000
New Car	$3,900	$26,000
Gallon Gas	$0	
Eggs, dozen	$0	
Postage Stamp	$0.04	$0.41
Burger	$0.20	$0.99

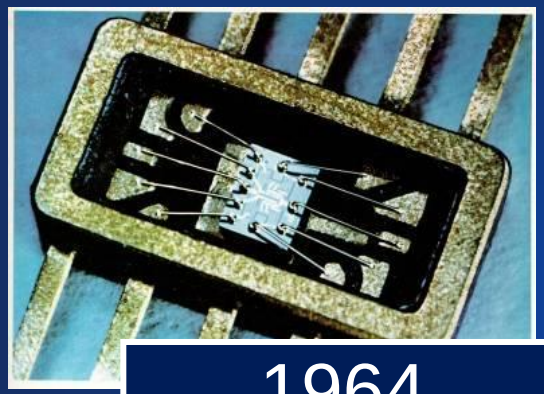
But NOT for semiconductors !



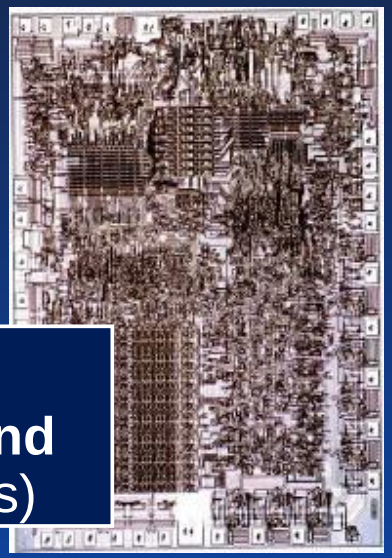
To our knowledge, no other industry has achieved such progress.

It was done by shrinking CMOS transistors to **near-atomic dimensions** and controlling purity to **parts per billion** — all on silicon wafers the size of a pizza.

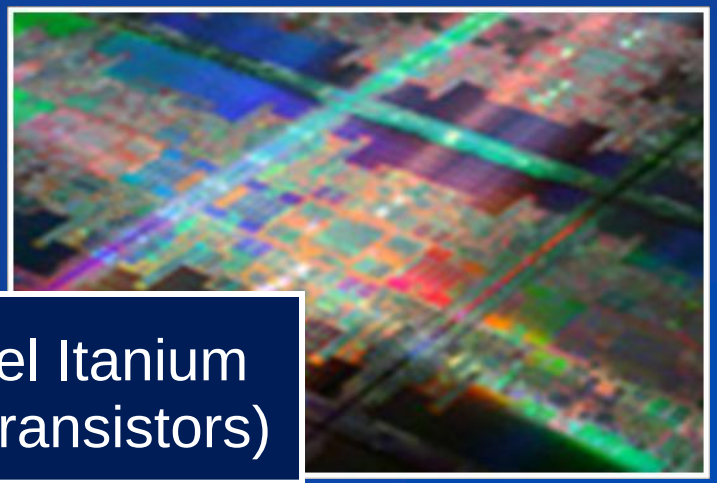




1964
(3 transistors)



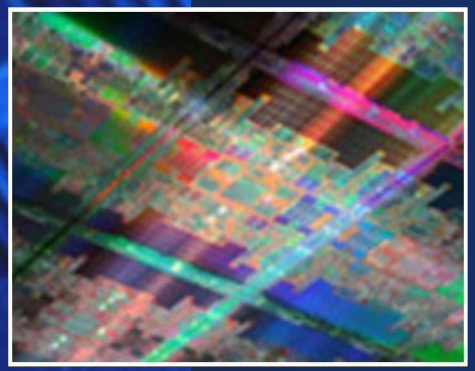
1974
(5 **thousand** transistors)

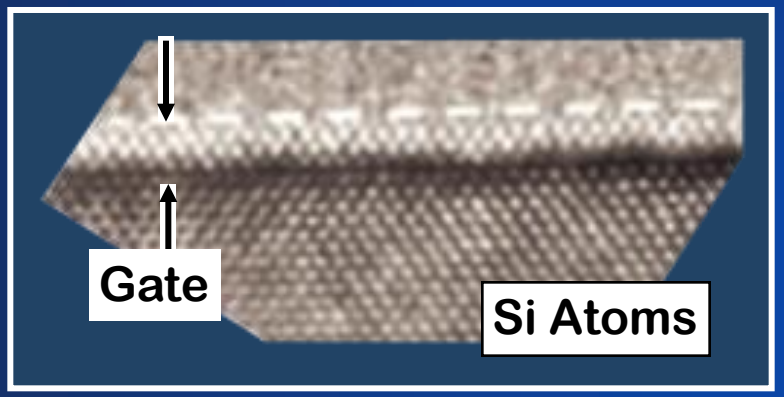


2008 Intel Itanium
(2 **billion** transistors)

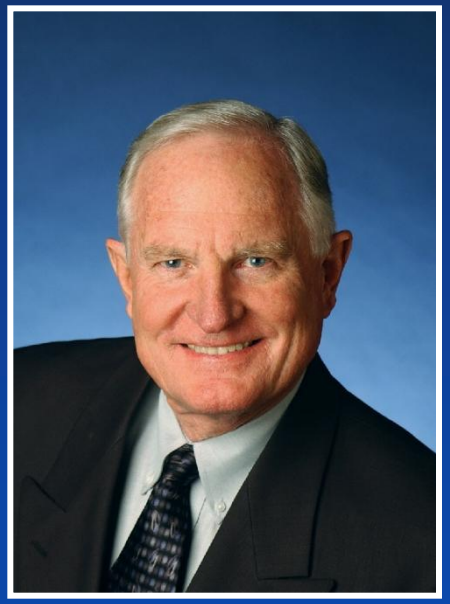
"You're Crazy"

"I still look at these circuits of **2 BILLION transistors** … and I ask myself, "What's the probability that 2 Billion of these things will **ALL** work? ... The gate is (only) **five molecules thick** … And you say, "You're crazy. Nobody can make these things. It's not going to work." But they do work … (and) you can crank out millions of these devices."





Magnification ~ 7 Million

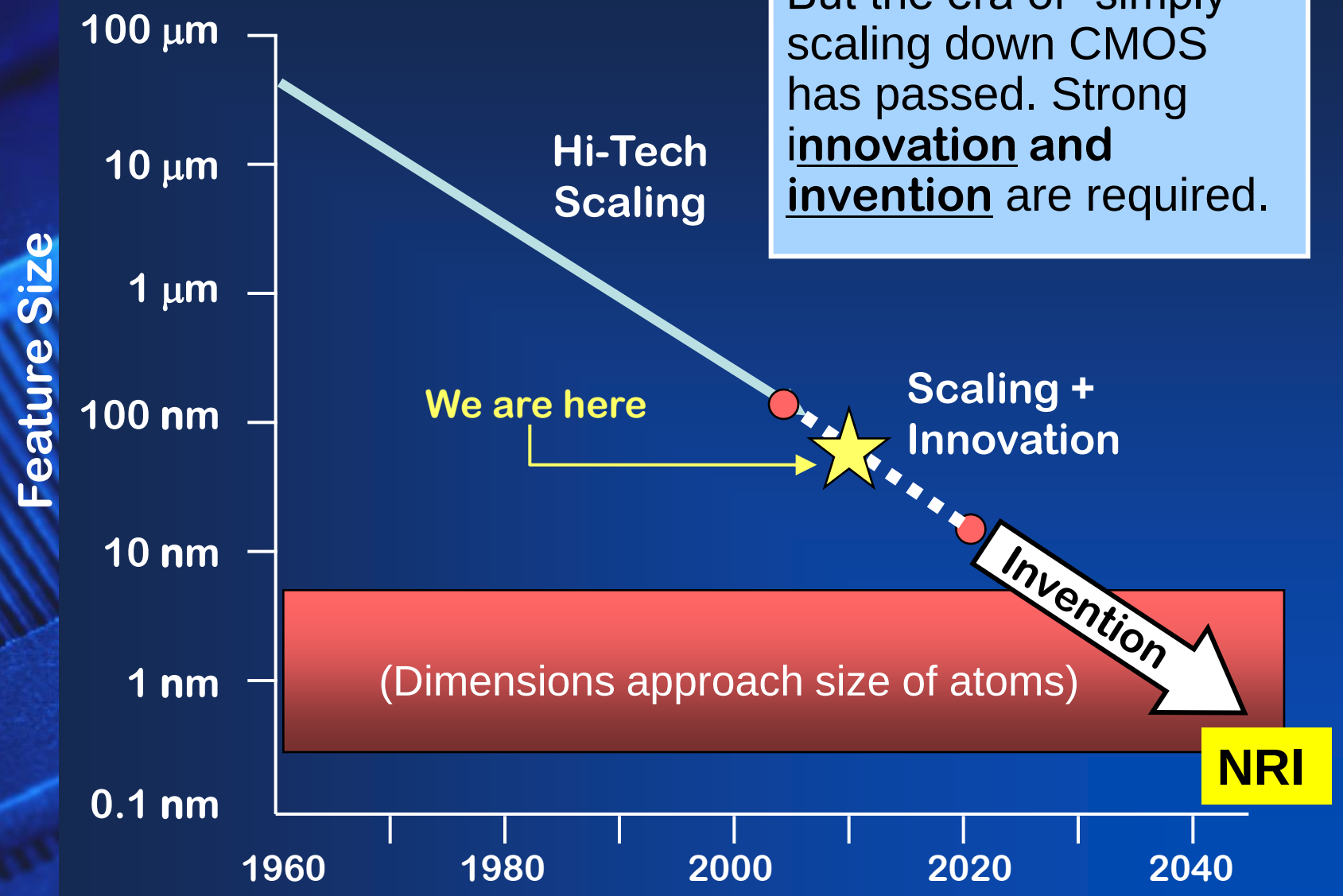


Dr. Craig Barrett
Chairman
Intel Corp.

IEEE Design & Test, July/Aug 2008

Trouble Ahead

But the era of "simply" scaling down CMOS has passed. Strong **innovation and invention** are required.



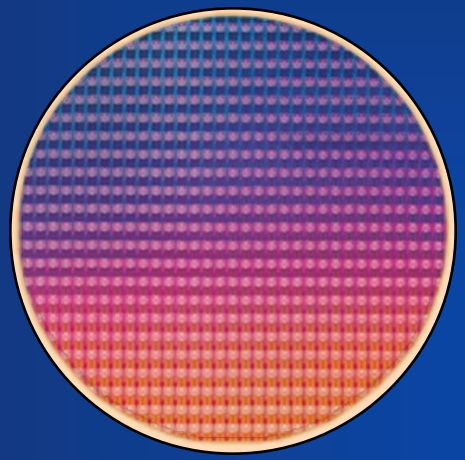
After J. Plummer, Stanford Univ.

NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

It will have to **meet** the many desirable properties of CMOS devices, but **sidestep** their limitations.

Size

Cost



Speed

Heat Generation

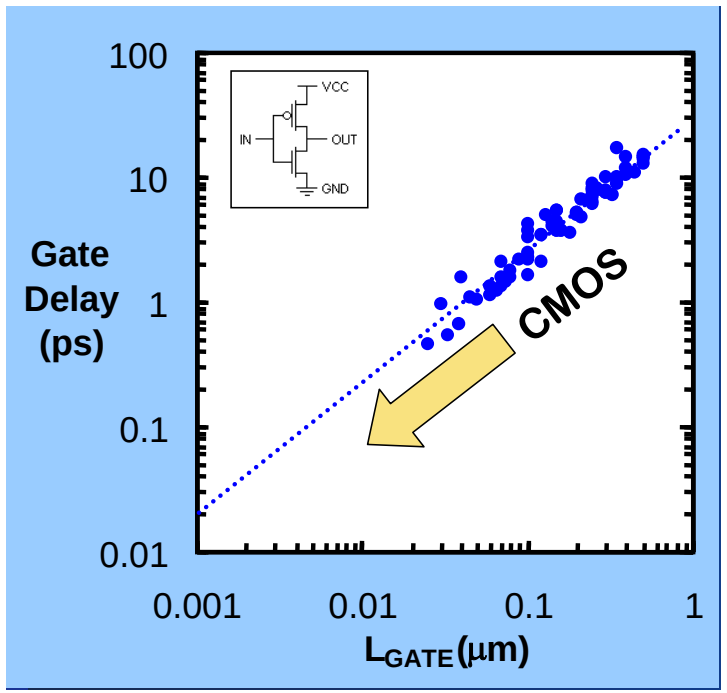
Power Consumption

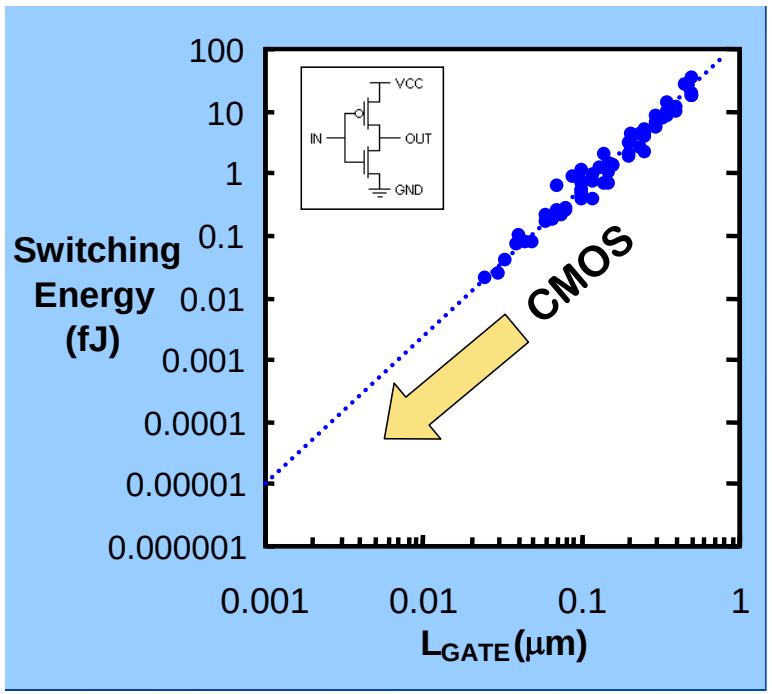
CMOS Limitation # 1 — Size

It is important to continue shrinking device dimensions:

- To further increase speed and reduce switching energy
- To increase functionality and reduce manufacturing cost per bit

But as gate dimensions approach **atomic size**, tunneling and quantum effects degrade device operation.

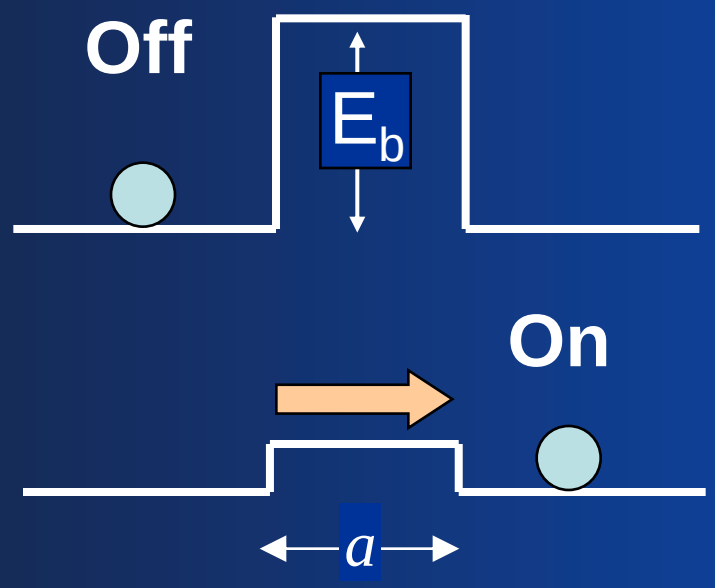




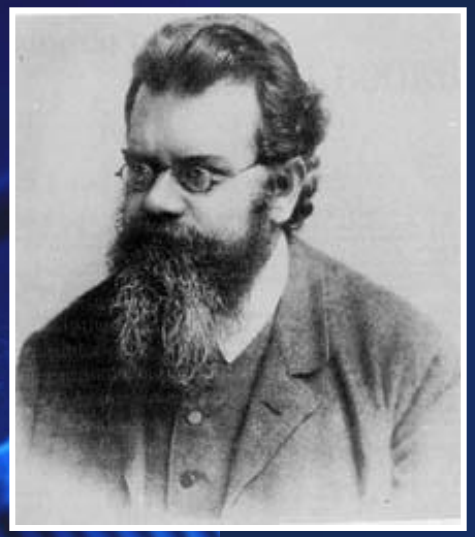
Lessons from the Past

By applying **fundamental** laws of solid-state physics and quantum mechanics, we can estimate the **limits** of size, speed and energy dissipation for electron switching devices.

Two-Well Electron Switching Model



Basic Physics



From the **Boltzmann distribution**, the minimum energy barrier to differentiate between two electron states is:

$$E_b = kT\ln 2$$

From **Heisenberg's position-momentum** principle, the minimum spacing of 2 states is:

$$a_{\min} \approx \frac{\hbar}{\sqrt{2mE_b}}$$

From **Heisenberg's energy-time** constraint, minimum traversal time between 2 states is:

$$t_{\min} \approx \frac{\hbar}{E_b}$$

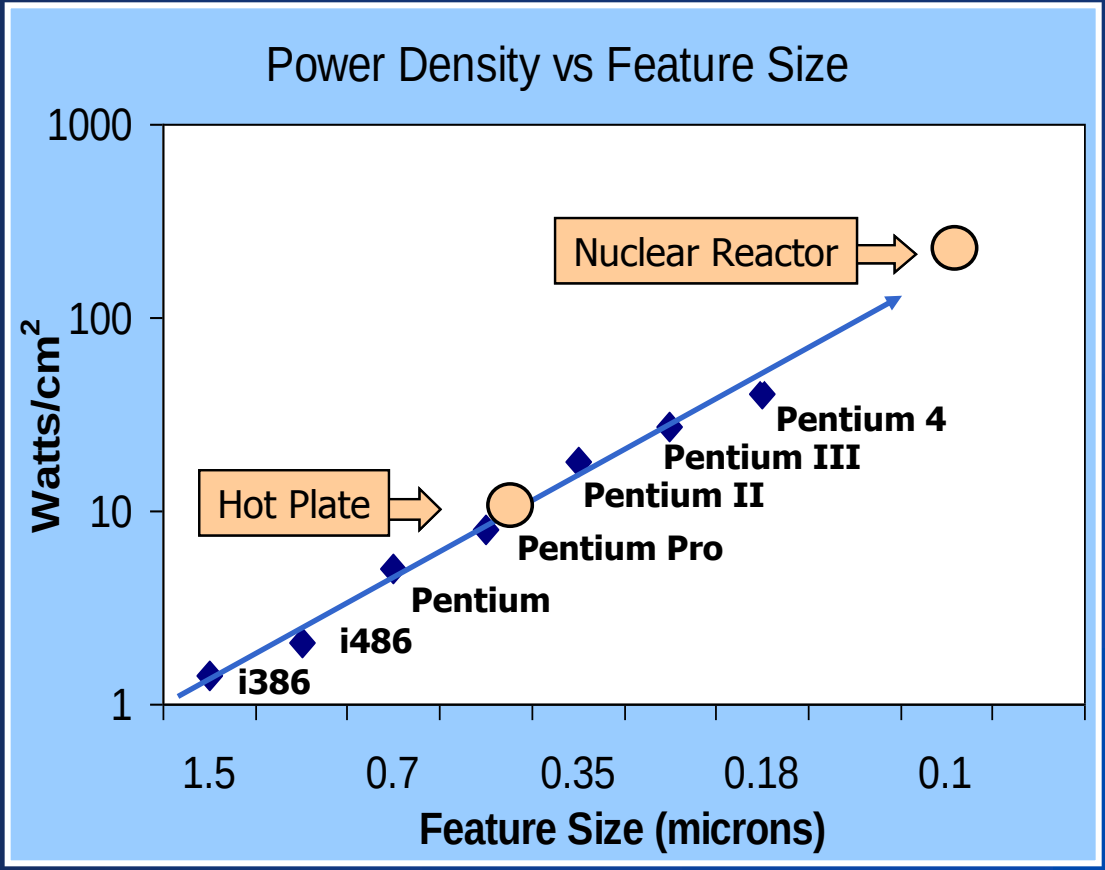
Calculated Limits

	Limiting Physics	Value (at 300°K)
Minimum Energy per Binary Transition	Boltzmann Constraint	3×10^{-21} joules OK
Minimum Separation of 2 Distinguishable States	Heisenberg Uncertainty	**5 nm** ~~1.5 nm~~ X
Minimum State Switching Time	Heisenberg Uncertainty	4×10^{-14} sec OK
Maximum Gate Density	$1/a^2$	5×10^{13} gate/cm² OK

In practice, for the electron states to be highly distinguishable and to avoid tunneling, the minimum separation climbs to ~ **5 nm** !

CMOS Limitation # 2 — Heat

As dimensions continue to shrink, high-performance ICs will generate inordinate amounts of heat — **to the point of self destruction!**



Circuit Power Dissipation

We can calculate the total device **power dissipation by using the physical limits described earlier:**

$1/(1.5\text{nm})^2 \sim 10^{13}\ \text{cm}^{-2}$ $\quad k_B T \ln 2 \sim 10^{-21}\ \text{J}$

$$\text{Power} = \frac{\text{Gate Density x Energy per transition}}{\text{Switching time}}$$

$h/k_B T \ln 2 \sim 10^{-14}\ \text{s}$

Power = 5 Megawatts ✗

The device will vaporize!

Heat Removal

Current methods to remove heat from IC chips are about **5,000** times less than this.

	Value
Thermoelectric	680 W/cm^2
Micro-channel	790 W/cm^2

NRI Vector: NEW METHODS TO MANAGE HEAT

New Approaches in Nanoelectronics

The limits on **size** and **heat dissipation** for CMOS beyond ~ 2020 have prompted researchers to pursue dramatically **different approaches**.

Examples include:

- Alternative electron switching schemes
- Electron spin
- Architectures — Energy-Efficient Systems

ITRS Emerging Research Device Technology Candidates Evaluated

In 2008 ITRS ERD selected the following subset of device concepts for detailed evaluation:

- Nano-electro Mechanical Switches
- Collective Spin Devices
- Spin Transfer Torque Devices
- Atomic/Electrochemical Metallization Switch
- **Carbon-based Nanoelectronics**
- Single Electron Transistors
- CMOL / Field Programmable Nanowire Interconnect (FPNI)

Selected in 2008 for increased research emphasis

How can we go below 5 nm?

From Heisenberg (and Boltzmann) we learn that the minimum spacing of two particles is **inversely** related to their mass.

$$L^2 m = \text{Constant}$$

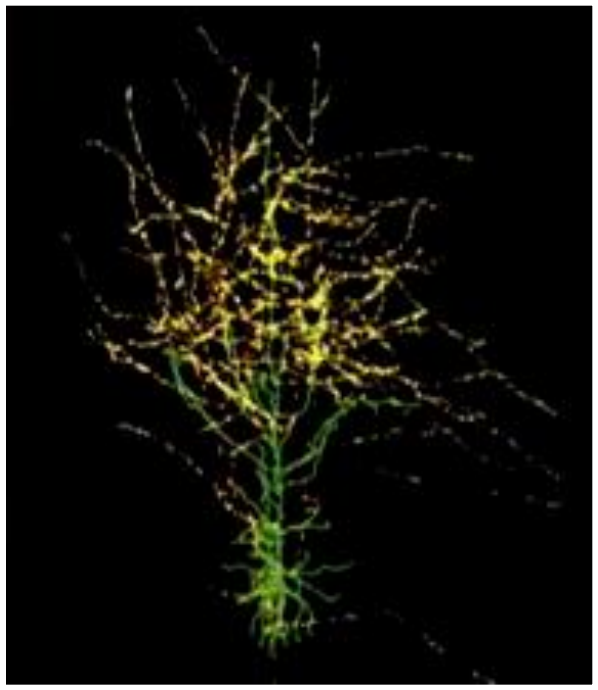
For spacing below ~ 5 nm, we should explore information carrying particles whose mass is greater than that of an electron.

e. g.,

- Move **atoms or molecules** instead of **electrons**
- **It appears that nature has successfully employed this idea**

Biological Information Processing

Ions in liquid electrolytes play an important role in biological information processors, such as the brain.

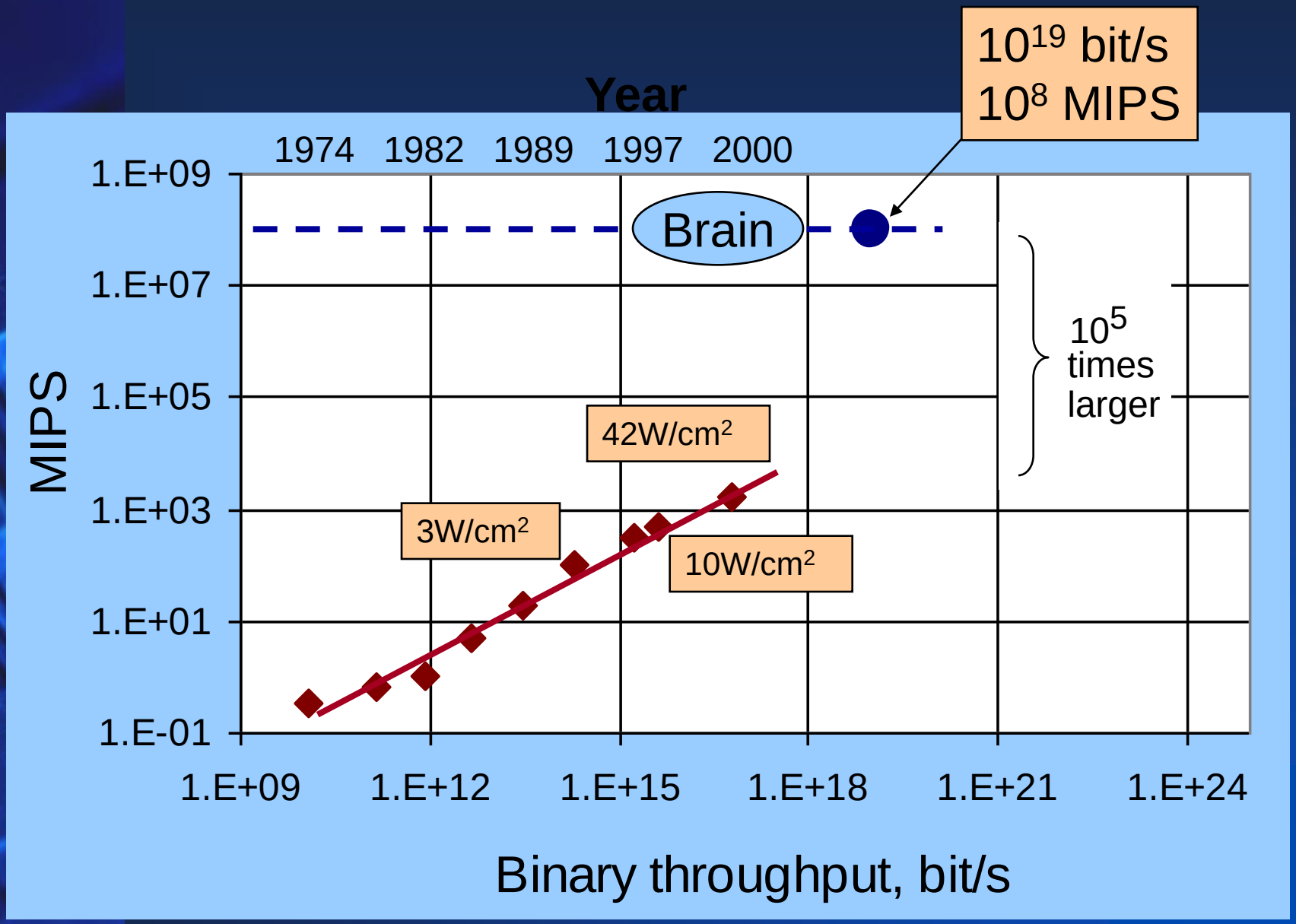


e.g., the distribution of Ca ions in dendrites is used for processing and storing information in the brain.

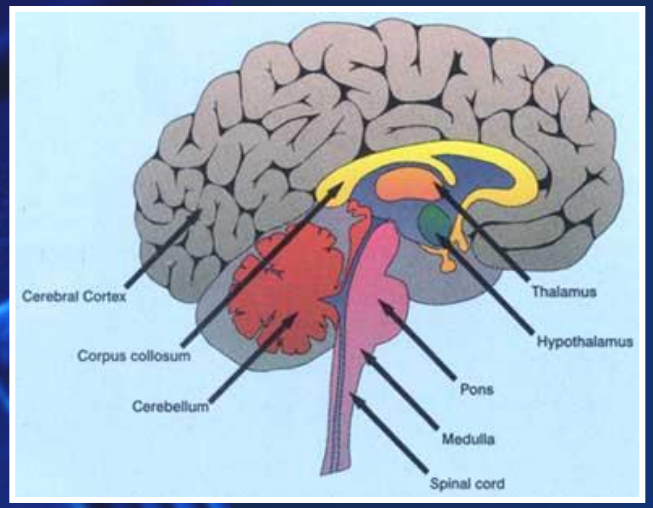
Ca ions enter the dendrites through voltage-gated channels.

Ions are heavy, but the brain has learned to use them efficiently!

Silicon vs. the Brain



Most Complex Processing System



	Dell 8250 (Pentium 4)	Hu B
Mass	~ 25 Kg	1
Volume	34,200 cm^3	1,3
MIPS	10^3 MIPS	10^8
BIT	< 10^{16} bit/s	10

A CMOS machine near the limits of scaling would use vast amounts of power

The processing capability of the brain is 10^5 times greater than a Pentium 4. If we multiply the power of the PC by this factor, we would need 20 Megawatts of power.

Brain vs. Computer

Garry Kasparov (World Chess Champion) vs. IBM

IBM's "Deep Blue"

- 32 Nodes
- 8 dedicated chess processors per node (total 256)
- 1.4 tons (lots of ac)
- **200 million positions analyzed per second**

Results

1996 – Feb. 10

- Kasparov – 3 wins, 2 draws
- Deep Blue – 1 win, 2 draws

Winner

Kasparov, 4 - 2

Rematch (after major computer upgrades and adjustments between games to "learn" from Kasparov's previous moves)

1997 – May 11

- Kasparov – 1 win, 3 draws
- Deep Blue – 2 wins, 3 draws

Winner

DEEP BLUE, 3½ - 2½

"Assembly"

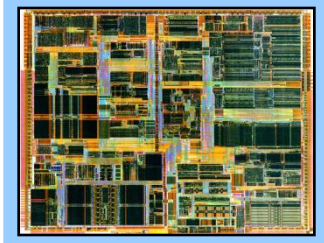
Complex Matter = Energy + Information + Material

IC Chip

Light, e-beam

10001100110010
Mask

Silicon



Waste

ENERGY

INFORMATION

MATERIAL

Living Organism

Food
Oxygen

DNA

13244242424
14232341324
23234122431
14235142323
23231423212

Amino Acids, Proteins

Waste

Growth of a Human Embryo

A new human is "assembled" very efficiently, compared to a semiconductor chip.

Weight of Fully "assembled" Fetus	3 kg
Additional Energy Needed (by mother)	300 per day
Assembly Time	9 months
Total Assembled Molecules	5×10^{25}
Assembly Rate	2×10^{18} molecules/sec

The "assembly rate" for a human fetus is about **10^8 times greater** than for a semiconductor chip.

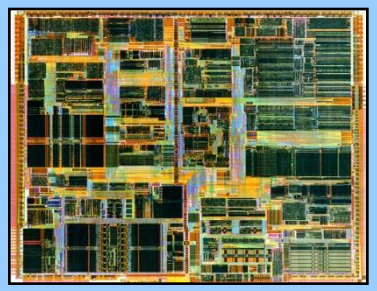
Other Differences

Living Organisms

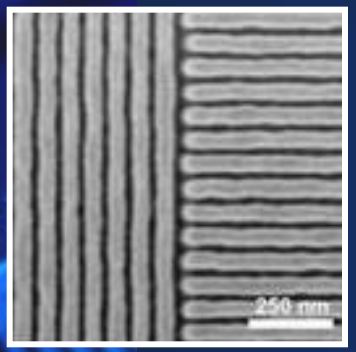
- Entirely **additive** processing
- Few-of-a-kind processing

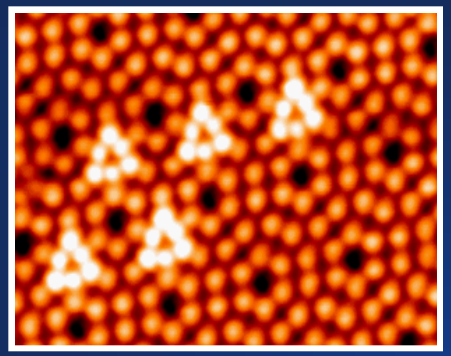
Semiconductors

- Combination of **additive** (deposition) and **subtractive** (etching) processing
- Mass production of thousands of identical ICs



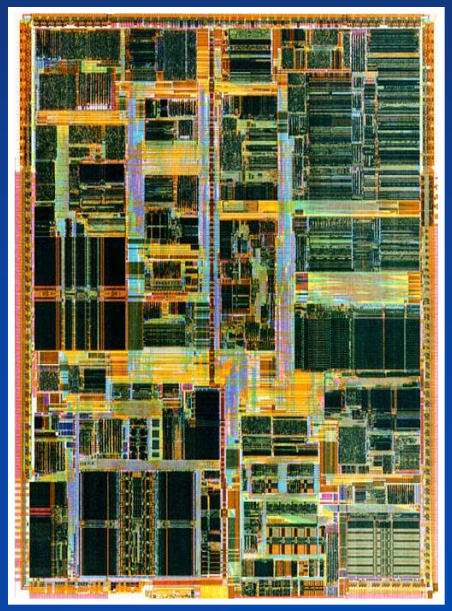
Self Assembly





Self-assembly today is in its infancy, producing small patterns of simple elements in exotic polymers.

But … we need very complex structures of electrically active devices.



NRI Vector: Self Assembly for devices

Nanotechnology Convergence

Nanoelectronics

Quantum Mechanics

- What are the fundamental physical limits of binary switches?

Thermodynamics

- What are the fundamental limits of heat removal?

Biology & Chemistry

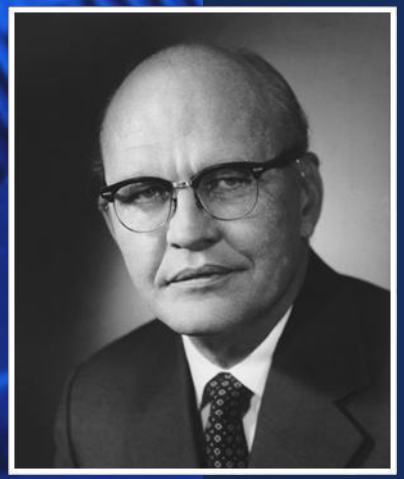
- Can we 'teach' matter to organize into desired structures?

NRI relies on fundamental science

Summary

The advances in electronics over the past 60 years stem from the discoveries of a handful of scientists …

- Maxwell, Heisenberg, Boltzman, Einstein, Bohr, et. al. – who described the world of solid-state physics
- John Bardeen, Walter Brattain & William Shockley, who applied their laws to build a transistor



- Jack Kilby, who first combined a few of these tiny specks into an integrated circuit.

Summary

Subsequent advances were made by an **ARMY** of dedicated technologists.

- Their efforts have extended of solid-state physics to all aspects of modern civilization.
- **BUT**, we're approaching the end of our tracks. We again need **highly creative scientists** to overcome **fundamental** limitations.
- This is the quest NRI has undertaken! – Ideas are welcome.

Nanoelectronics Research Initiative (NRI) Vectors

NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

To meet these goals, NRI pursues five research vectors:

- **NEW DEVICE:** Device with alternative state vector
- **NEW WAYS TO CONNECT DEVICES:** Non-charge data transfer
- **NEW METHODS FOR COMPUTATION:** Non-equilibrium systems
- **NEW METHODS TO MANAGE HEAT:** Nanoscale phonon engineering
- **NEW METHODS OF FABRICATION:** Directed self-assembly of devices