Collective Computation with Self Assembled Quantum Dots, Nanowires and Nanodiodes: A Novel Paradigm for Nanoelectronics

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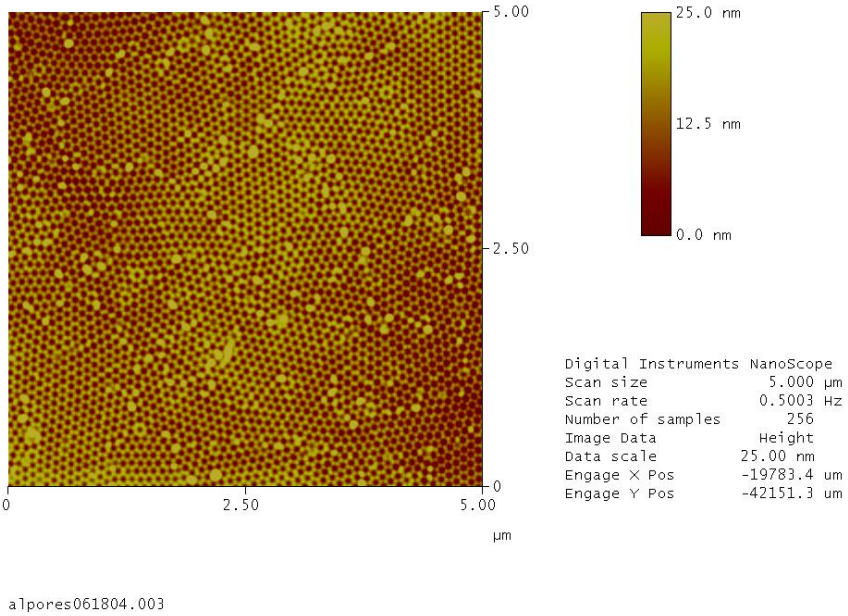
PIs: **Supriyo Bandyopadhyay, Koray Karahaliloglu, Pinaki Mazumder and Kang Wang**
Virginia Commonwealth University, University of Michigan-Ann Arbor, UCLA

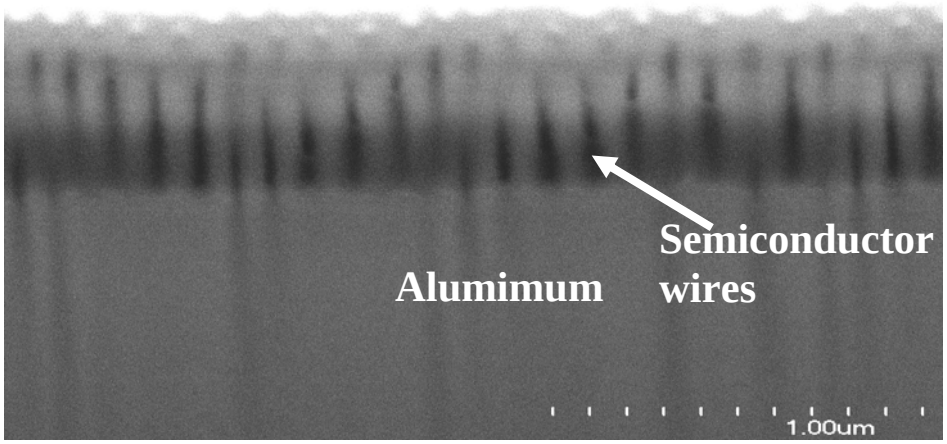
The workhorse of modern electronics is the ubiquitous "transistor" that serves as the primitive unit for all signal processing and computational functions. As the transistor dimensions shrink, a host of problems begins to emerge, such as gain degradation, loss of isolation between input and output, threshold variability and exponentially burgeoning costs.

To mitigate these problems, we began to look at alternate paradigms for computation and signal processing that bypassed the transistor and instead employed two-terminal non-linear devices to elicit useful computational functions. Ten years ago, we theoretically demonstrated that a two – dimensional array of nanowires, each exhibiting a negative differential resistance, and each linked to its nearest neighbors via resistive and/or capacitive coupling, can serve as associate memory, Boolean logic processors and perform such complex tasks as combinatorial optimization and image processing [1-3]. The only requirement was that the conduction through the nanowires should exhibit a negative differential resistance.

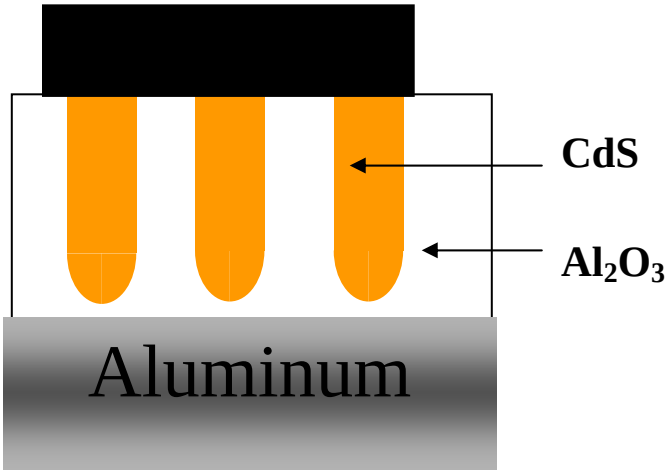
This array was self assembled electrochemically by electrodepositing a semiconductor within 50-nm diameter pores of an anodic alumina film. An AFM micrograph of the film is shown below.

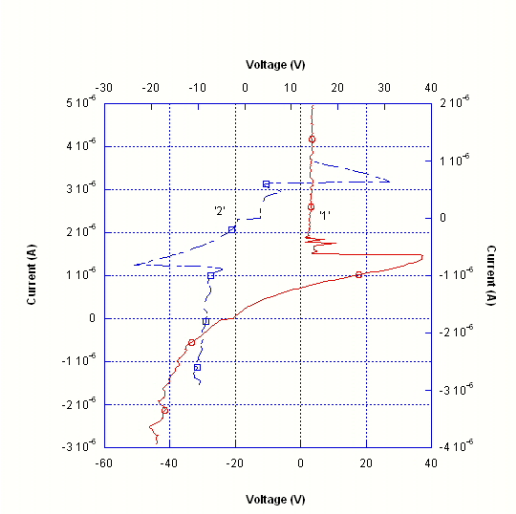


A typical cross-section TEM micrograph of wires selectively deposited in the pores is shown in the next figure. These structures replicate a metal-insulator-semiconductor diode and therefore each nanowire exhibits an S-type current voltage characteristic at room temperature.

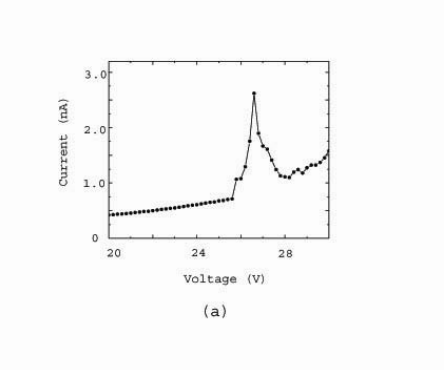


In the figure below, we show the schematic cross section of the self assembled structure and the measured current-voltage characteristic of the nanowires.





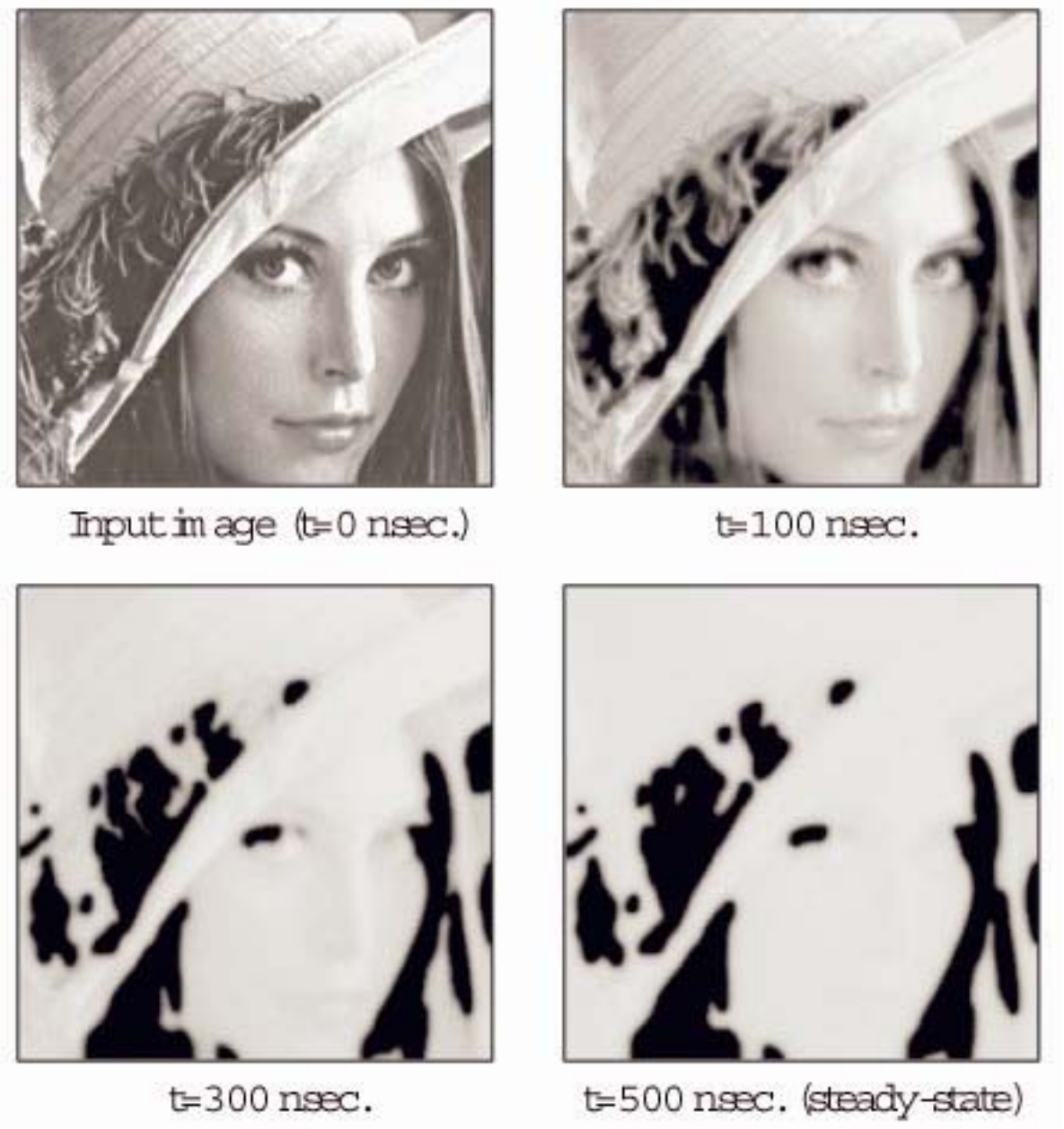
The measured peak to valley ratio of the negative differential resistance is 19:1 at room temperature.



We have also observed N-type negative differential resistance in some nanowires as shown alongside. The peak to valley ratio here is only 2.5: 1, but is still adequate for some functions such as image processing.

We have simulated a scenario where pixel intensities of an input gray scale image (8-bit greycode) are mapped on to the voltage states on the nanowires. *The electrical parameters assumed in the simulation (inter-wire capacitance, peak to*

valley ratio, interwire resistance, etc.) all correspond to experimentally measured quantities. The system is allowed to relax in time and the final steady state voltages correspond to a processed image where the processing leads to edge enhancement detection as shown below.



References

1. V. P. Roychowdhury, D. B. Janes, S. Bandyopadhyay and X. Wang, IEEE Trans. Elec. Dev., 43, 1688 (1996).
2. V. P. Roychowdhury, D. B. Janes and S. Bandyopadhyay, Proc. IEEE, 85, 574 (1997).
3. K. Karahaliloglu, S. Balkir, S. Bandyopadhyay and S. Pramanik, IEEE Trans. Elec. Dev., 50, 1610 (2003).