

## NANO HIGHLIGHT

### Highly Effective Digital Architectures for Hybrid CMOS/Nanodevice Circuits

NSF NIRT Grant 0403618

PIs: Konstantin K. Likharev (PI), James E. Lukens (Co-PI), Andreas Mayr (Co-PI)  
 Stony Brook University

Our analytical calculations and Monte Carlo simulation indicate that digital memory and logic circuits based on the hybrid CMOS/nanodevice (“CMOL”) concept [1, 2] may extend the Moore Law well beyond the 10-nm frontier. Indeed, we have shown [3, 5] that CMOL memory circuits using a combination of bad bit exclusion and advanced error-correction codes, enable terabit-scale integration with high defect tolerance (up to 10% of bad devices) and high (nanosecond-scale) speed. We have also shown [5, 6] that for that for a common benchmark (so-called “Toronto 20”) set of digital circuits, our FPGA-like approach [4] to CMOL logic circuits allows to obtain the average delay-area product approximately two orders of magnitude lower than that of purely-CMOS FPGA circuits (with the same design rules), at high (> 20%) defect tolerance and ITRS-specified power consumption. We believe that these findings give a strong motivation for the practical development of CMOL technology.

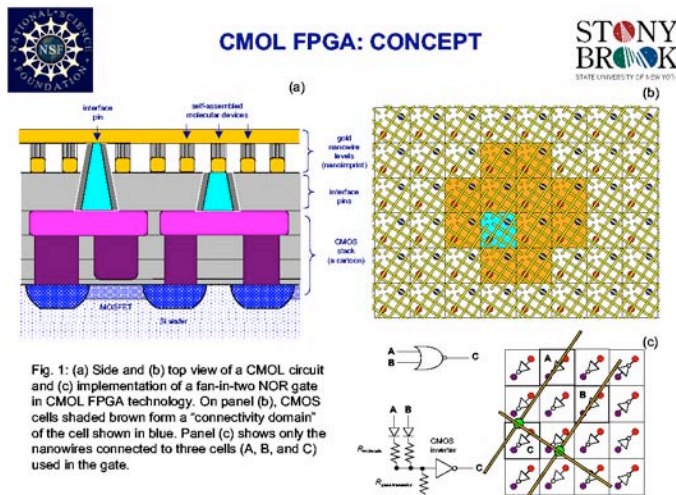


Fig. 1: (a) Side and (b) top view of a CMOL circuit and (c) implementation of a far-in-two NOR gate in CMOL FPGA technology. On panel (b), CMOS cells shaded brown form a “connectivity domain” of the cell shown in blue. Panel (c) shows only the nanowires connected to three cells (A, B, and C) used in the gate.

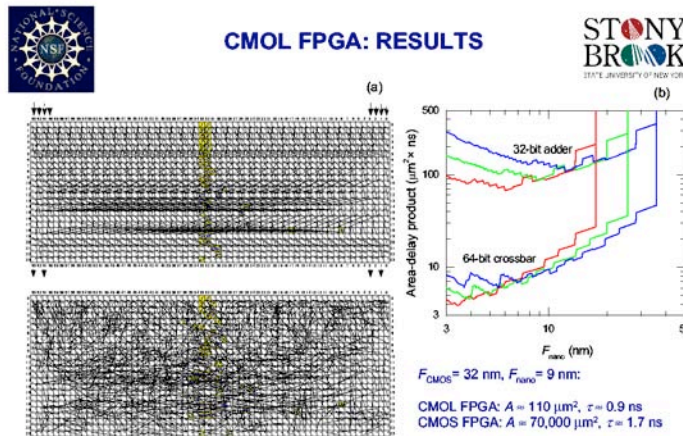


Fig. 2: A representative logic circuit (32-bit Kogge-Stone adder): (a) mapping on CMOL FPGA fabric before and after reconfiguration around as many as 50% of randomly located bad nanodevices, and (b) performance optimization results.  $F_{\text{CMOS}}$  and  $F_{\text{nano}}$  are half-pitches of, respectively, the CMOS and nanodevice/nanowire subsystems.

#### References:

- [1] K. K. Likharev, *Interface* **14**, No. 1, 43 (2005).
- [2] K. K. Likharev and D. B. Strukov, “CMOL: Devices, Circuits, and Architectures”, in: G. Cuniberti *et al.* (eds.), *Introducing Molecular Electronics*, Springer, Berlin (2005), pp. 447-477.
- [3] D. B. Strukov and K. K. Likharev, *Nanotechnology* **16**, 137 (2005).
- [4] D. B. Strukov and K. K. Likharev, *Nanotechnology* **16**, 888 (2005).
- [5] A. DeHon and K. Likharev, “Hybrid CMOS/Nanoelectronic Digital Circuits: Devices, Architectures, and Design Automation”, in: *Proc. ICCAD’05*, pp. 375-386.
- [6] D. B. Strukov and K. K. Likharev, “A Reconfigurable Architecture for Hybrid CMOS/Nanodevice Circuits”, accepted for presentation at *FPGA’06* (Monterey, CA, Feb. 2006); available online at <http://rsfq1.physics.sunysb.edu/~likharev/nano/FPGA06.pdf>

For further information about this project see <http://rsfq1.physics.sunysb.edu/~likharev/nano/>