Nanoarrays of large bandgap semiconductors for light emitting and spintronic applications

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A critical issue in III-Nitride materials is crystal quality. Because device layers are currently grown on foreign substrates, threading dislocation densities are extremely high, 10^7 to 10^9 cm^{-2}. These defects reduce minority carrier lifetimes and, subsequently, radiative emission. One evolving approach to alleviating this problem is to prepare nanowires of GaN which can, in principle, be highly perfect.

We have conducted preliminary experiments forming Ni nanodots on Si and Al_2O_3 substrates, and GaN epitaxial layers [1]. A layer of nickel, 3 nm thick, was deposited on Si(111) using an electron-beam evaporator, without removal of the native oxide of Si. Unlike previous studies of self-assembly in which metal films were deposited at a high substrate temperatures, only room temperature deposition, without intentional heating, was used in our experiments. We rely on precise control of the initial layer thickness and careful post-deposition annealing to control the size and density of Ni nanodots.

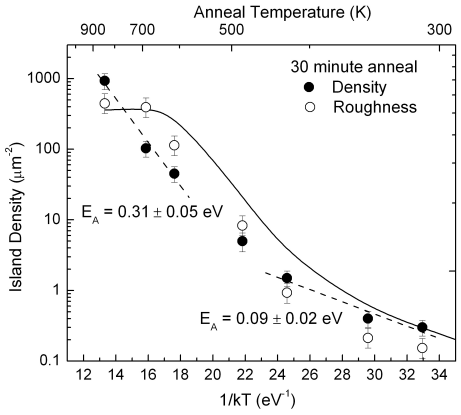

Fig. 1 Arrhenius plot of island density (●). Activation energies are obtained from fits to the data in the low and high anneal temperature ranges (dashed lines). The RMS roughness evolution is also shown (○). The solid curve is calculated RMS roughness based on the density and uniform nanodot shapes.

AFM measurements of as-deposited Ni films show very smooth surfaces, with $\sigma_{RMS} < 1$ nm. The AFM images were obtained following 500ºC annealing within 1 h of annealing; nanodots relax from rectangular to dome shapes after ~1 h. The anneals produced nanodots with truncated trapezoidal shapes with lateral dimensions 180 nm × 260 nm and average thickness of 16 nm.

Two aspects of 500°C anneals are interesting. First, the density of nanodots (n) increases with the anneal time. Second, their size and shape does not depend strongly on anneal time. We observe a direct dependence of the nanodot density n on anneal time $n \propto t^{\beta}$ ($\beta = 1.13 \pm 0.12$). The island density n was found to increase with anneal temperature. Fig. 1 shows an Arrhenius plot of island density. The density dependence is consistent with two activation energies, $E_A \sim 0.09 \pm 0.02$ eV obtained for low anneal temperatures, and $E_A \sim 0.31 \pm 0.05$ eV obtained at higher temperatures. These activation energies are relatively low, suggesting surface diffusion as a likely mechanism for Ni nanodot formation. Literature values of Ni self-diffusion, across major crystal facets, provide E_A (111) = 0.063 eV, E_A (110) = 0.39 eV, and E_A (100) = 0.68 eV. Our measured E_A results are in agreement with the calculated values for surface self-diffusion of Ni on (111) and (110) surfaces. The formation kinetics of nanodots is thus consistent with diffusion-driven growth across primarily these two crystal facets. These are the surfaces evolving on our

truncated huts imaged the AFM analysis. At the highest temperature studied in Fig. 1, the nanodot size is found to drop significantly to ~ 30 nm in diameter, and the density is seen to rise dramatically. Thus, on Si(111) substrates, these preliminary studies provide important information about the preparation of high-density Ni nanodots.

Root-mean square (RMS) roughness values (σ_{RMS}) obtained from the AFM measurements are also shown in Fig. 1. Since our nanodots are well described as nearly identical structures (height h and area A_0), with the primary variable being the island density, an analytical relationship between σ_{RMS} and n is derived

$$\sigma_{RMS}^2 = \frac{1}{A}\iint_A (z(\mathbf{r}) - \bar{z})^2 \, d\mathbf{r} \rightarrow nA_0(1 - nA_0)h^2 \qquad (1)$$

where z is the height at position $\mathbf{r}$ = (x,y). The solid curve in Fig. 1 is the result of this calculation, showing excellent agreement with the RMS data.

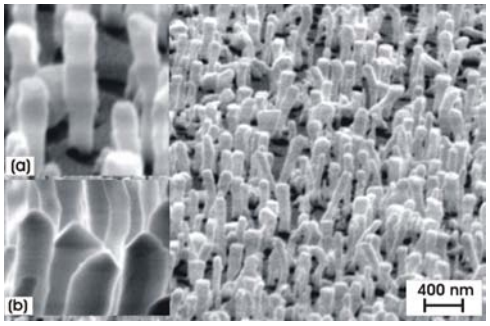

Fig. 2. SEM images of GaN nanowires. (a) high magnification image of a wire 100 nm in diameter. (b) metal caps on nanowires.

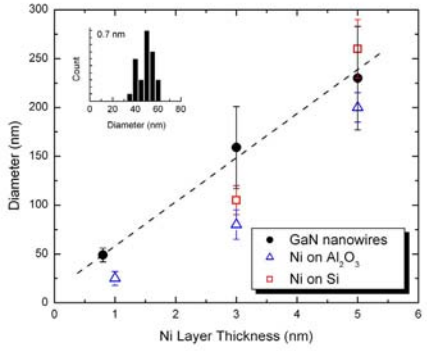

Fig. 3. GaN nanowire and Ni nanodot diameter vs. initial Ni thickness on sapphire. Inset: diameter histogram (0.7 nm Ni).

We have used these studies to form Ni nanodots on sapphire substrates. At the annealing temperature of 830ºC, used in the growth of GaN nanowires, the nanodot size is ~ 80 nm and is very uniform.

We have recently investigated growth experiments of GaN nanowires using the vapor-liquid-solid (VLS) approach. Thin layers of Ni, from 0.5 to 3 nm, are evaporated onto a substrate and GaN nanowires are grown on sapphire substrates by MOCVD [2]. SEM images of GaN nanowires are shown in Fig. 2. These nanowires grow with c-axis perpendicular to the substrate, with fairly constant diameters, smooth sidewalls, and hexagonal cross-sections. Nanowires grow selectively from islands of the metal catalyst and no deposits of GaN could be seen between the wires. A slight increase in the diameter of the growing wire, Fig. 2(a), may be indicative of sidewall growth. Characteristic metal caps at nanowires tips, Fig. 2(b), confirm the VLS mechanism of their formation. The shape of the caps is typical of Ni nanodots formed in high temperature, 830°C, anneals.

Control over the diameter of the nanowires has been achieved over a broad range. Fig. 3 correlates GaN nanowire diameter vs. initial Ni layer thickness. Also shown are the diameters of Ni nanodots formed on both Si and sapphire substrates. There is a clear correlation between Ni nanodot diameter and that of the GaN nanowire. This permits control of the diameter of GaN nanowires. By varying growth time, we can produce nanowires with controlled length, up to 2 μm.

Nanotextured Surfaces for Sensor Components. We are experimenting with sophisticated nanotexturing of surfaces for the control of optical properties. One specific application is

increasing LED extraction efficiency. In our demonstration, Si is plasma etched to produce an array of holes having diameter ~ 60 nm and varying depth up to 2 μm [3]. Initial work has focused on the use of self-assembled templates in alumina, which we present here. We are now experimenting with electron-beam lithography and block copolymers for producing structured arrays. SEM images of the patterned surface and a cross-section are shown in Fig. 4. In Fig. 5 we show the reflectance spectra across the 2 to 6 eV (620 to 206 nm) photon energy (wavelength) range [4]. Clearly seen is a systematic decrease in reflectance with nanopore depth, dropping below 50% that of the starting Si wafer across the entire photon energy range studied. Dashed curves show an effective medium model of the optical properties taking into account the small diffuse reflectance losses. Raman studies reveal that insertion and extraction efficiencies increase by factors of two in each case. The results suggest that nanotexturing the surfaces of semiconductor-based devices could have an important impact on the performance of LEDs and photodetectors operating in the UV, and consequently on the sensitivity of sensors based on them. There are also potential advantages based on the nanotexturing of surfaces for selective binding in chemical and biological sensors.

References

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