

Single Nanoparticle Devices, A New Technique for Bottom-Up Manufacturing

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The use of single crystal semiconductor nanoparticles for building electronic and optoelectronic devices would allow the construction of three-dimensional circuits and the integration of otherwise chemically and structurally incompatible single-crystal materials on a single substrate. Not only would this dramatically reduce interconnect delay in integrated circuits, the elimination of parasitic capacitances related to the use of silicon wafers could produce devices with switching speeds well in excess of 100 GHz. This NIRT will demonstrate the technologies needed to make such devices. Specifically the project will: 1) synthesize and characterize monodisperse aerosols of 30 to 100 nm, single-crystal silicon nanoparticles, 2) use electrostatics to assemble these nanoparticles at predetermined sites on a substrate, and 3) build and characterize high performance transistors using these nanoparticles.

The first goal, the production of highly perfect single crystal Si nanoparticles has been achieved using a constricted capacitively coupled plasma^{1,2,3}. The system uses a ring electrode around a 5 cm outer diameter discharge tube. Particles are extracted from the plasma through a 1-mm orifice and impacted on TEM grids that are located in a high vacuum chamber. Studies with a high-speed intensified video camera showed that the discharge was a striated, high-luminosity plasma filament that rotated close to the wall at ~150 Hz. This plasma was found to reproducibly produce the very well defined silicon single crystal nanocubes shown in Figure 1. The particles were highly monodisperse with a size

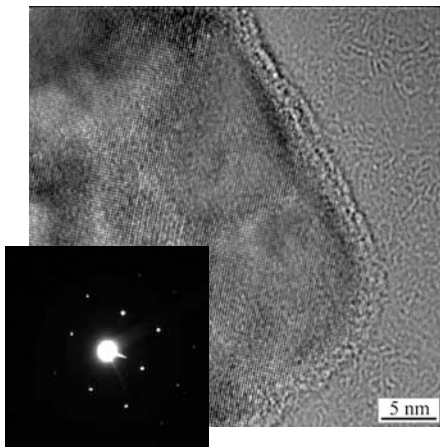


Figure 2 – C_s corrected HRTEM image. Insert shows selected area diffraction of the diamond structure and (001) faces.

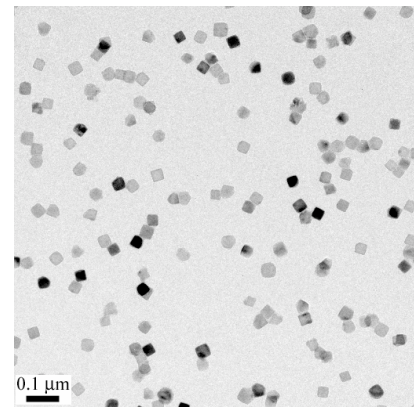


Figure 1: Single crystal, cubic shaped silicon nanoparticles produced in a nonthermal, constricted capacitive plasma.

distribution of a peak size of 35 nm and a standard deviation of 4.7 nm. TEM studies showed that the particles were perfect single crystals without twin boundaries or dislocations and had (100) faces. The particles had a thin amorphous surface layer. Elemental analysis of this layer showed it to be an oxide of silicon. Careful analysis of this oxide suggests that the clustering of particles seen in Figure 1 occurred after removal from the vacuum. High-resolution images of the particles were taken in Jülich, Germany using a spherical-aberration (C_s) corrected TEM. This allows one to distinguish the surface film from the amorphous support layer. As shown in Figure 2, the thin amorphous layer is a distinct, abrupt film which appears to be a native silicon dioxide film.

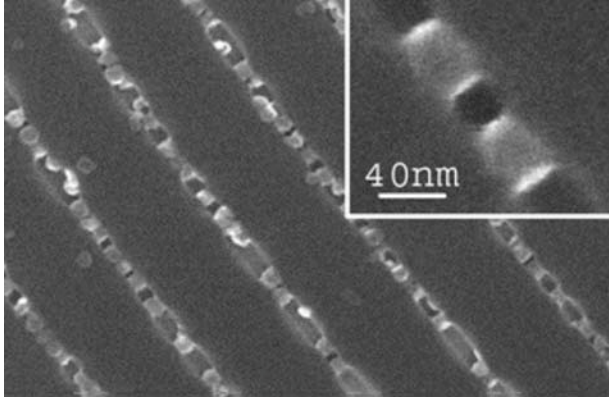


Figure 3 – Micrograph showing electrostatic localization of cubic nanoparticles using microstructure to assist the electric field.

To gain insight into the properties of the constricted plasma, we recently developed a simple plasma model. By performing an energy balance for the nanoparticles immersed in the plasma we found that the main heating mechanism is likely electron-ion recombination at the particle surface⁴. For the charge carrier densities expected in our plasma, this mechanism may lead to particle heating of several hundred Kelvin above the background gas temperature. We expect that this nonequilibrium of particle and gas temperature is essential for the efficient formation of silicon nanocrystals.

Professor Jacobs has developed a charge patterning process enabling nanoxerographic printing. The printing technique, referred to as electric nanocontact printing, generates a charge pattern based on the same physical principles used in scanning probes but forms multiple electric nanocontacts of different size and shape to transfer charge in a single step⁵. We have demonstrated charge patterning using flexible thin silicon electrodes and nanoxerographic printing which does not require a metal coating. Kelvin probing has been used to determine the charge pattern left in the electret. A major challenge for applying this approach to the single crystal nanoparticles has been the large kinetic energy of the particles as they pass through the critical orifice exiting the plasma chamber. After some effort, deceleration techniques have been developed and localization of the single crystal nanoparticles has been achieved. As shown in Figure 3, we have been able to achieve almost perfect alignment of these 40 nm single crystal particles. The technique to do this involves the use of fields created by resist coated field regions outside the developed lines.

Electrical characterization of nanoparticles has also been carried out. To do this, nanoparticles have been deposited on metallic or heavily doped silicon substrates. The particles were then embedded in an insulator. Chemical mechanical polishing and a blanket etchback were used to expose the top of the particles. Finally a top electrode was applied and patterned, forming a Schottky contact. Typical results are shown in Figure 4. By measuring the temperature dependence of these characteristics, we were able to determine three distinct regimes⁶. At low voltages, channel conduction along the faces of the nanoparticle was observed. Channels are formed due to the presence of positive charge in the insulator.

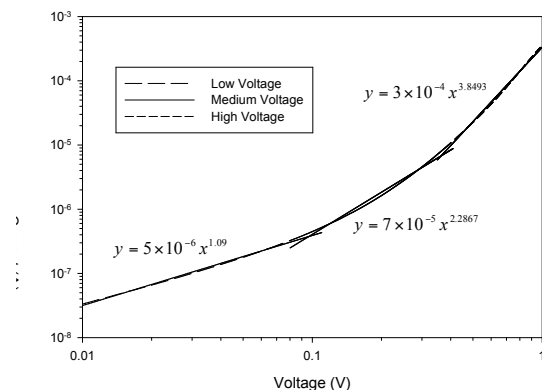


Figure 4 – Typical I-V characteristic through a single crystal nanoparticle showing three operating regimes.

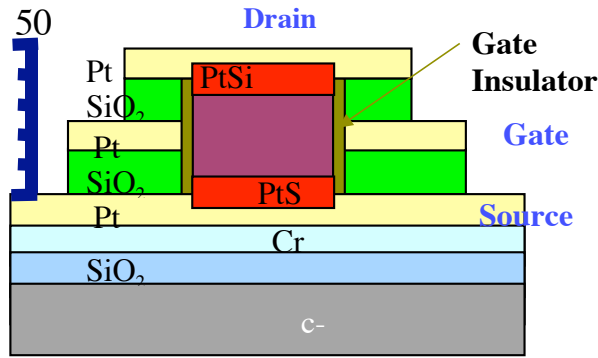


Figure 5 – Schematic of nanoparticle transistor showing all three terminals.

At moderate fields the current is determined by charge trapped at interface states on the surfaces of the nanoparticles. At the highest bias, double injection was observed. In this process carriers from the lower electrode receive enough energy traveling across the nanoparticle to create the opposite carriers at the upper electrode. Clearly control of the charge in the insulator and at the semiconductor/insulator interface will be a critical element of making successful nanoparticle devices.

The process used to make these metal-semiconductor-metal devices was then extended to a Schottky barrier, vertical flow field effect transistor. This is an extremely challenging proposition since, unlike nanotube devices, all three dimensions are only a few tens of nanometers. To do this a gate layer was inserted between the upper and lower electrodes by repeated deposition, polishing, and etchback steps. Figures 5 and 6 show the structure and the turn off characteristic. Although leaky, transistor action appears to have been observed with a gate turn off characteristic of ~ 70 mV/decade, in good agreement with theoretical values.

Significant work remains in all areas. Control of single crystal particle size has not been achieved. A system modification has been designed to accomplish this. While the localization results illustrate feasibility, the control of the system parameters needs to be improved. Currently we observe variation of the accomplished patterns between experiments. This may result from build up of charge on the insulating reactor walls. The transistor process also needs improvement as the devices are extremely leaky and very low yield. We are currently working in all of these areas and expect to make significant progress through the remainder of the funding period.

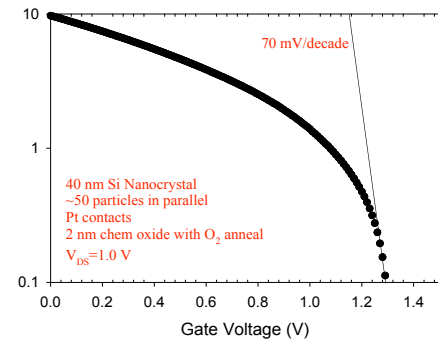


Figure 6 – I-V characteristics of nanoparticle device.

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