Optical Interconnects for High Performance Processors: Architectures, Circuits, and Devices

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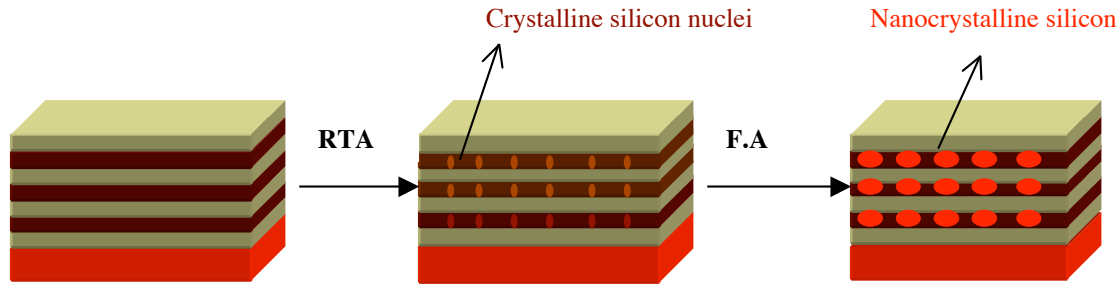
The International Technology Roadmap for Semiconductors (ITRS) identifies interconnect performance as one of the Grand Challenge problems facing the integrated circuit community in the long term (years 2008-2016). Global interconnect delays are predicted to increase by over a factor of five from the 130nm to the 45nm technology node (2010 timeframe). Relative to gate delays, global wire delays will increase by roughly a factor of 20 during this period. Techniques such as repeater insertion can mitigate this increase to some degree, but dramatically increase power dissipation. The ITRS further identifies optical technology as one of the prime candidates to solve the global signaling problem in future technology nodes.

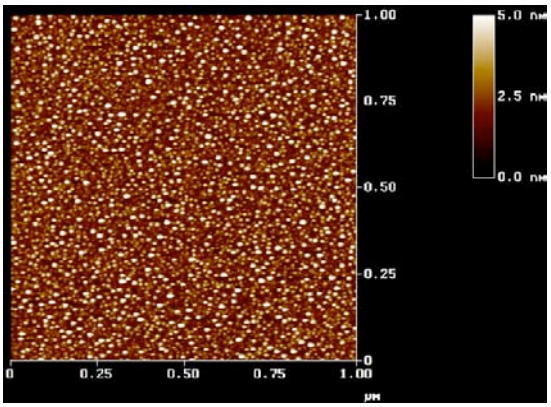
To date, most work on optical interconnects has focused on chip-to-chip interconnects, despite the urgent need to address the on-chip signaling problem. Indeed, skepticism exists as to even the long term viability of the use of optics for on-chip communication. This skepticism stems in part from the view that lasers must be constructed from non-silicon-based materials, such as III-IV compounds. The integration of such materials on random die locations for on-chip signaling presents a considerably challenging materials problem.

Our research at Rochester has focused on silicon at the nanoscale level, specifically in the areas of nanocrystalline silicon superlattices and porous silicon. We have made major strides towards the development of an all-silicon optical system, including light sources, switches, modulators, mirrors, and waveguides. An optoelectronic system based



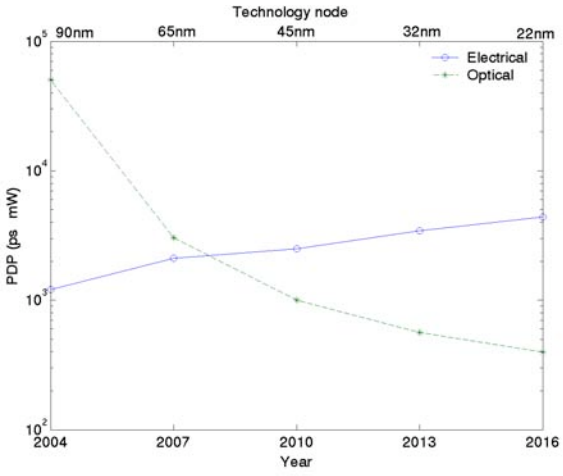
Cartoon representation of the steps used in the fabrication of the nanocrystalline silicon superlattices. After the rapid thermal annealing step which forms crystalline silicon nuclei, a gentler furnace annealing steps leads to the growth of quantum dots all having the same diameter given by the thickness of the initial silicon layer.

solely on silicon would have major ramifications across the semiconductor industry by circumventing the materials challenges associated with non-silicon optical devices. However, as with most nanotechnology research efforts, this work is exclusively focused on the design, fabrication, and characterization of individual devices. Little is known about how best to integrate such devices with CMOS, how the system should be architected to best exploit the speed and power advantages of silicon-based optical interconnects, and how silicon nanoscale devices should be fashioned to satisfy higher level requirements. There are also few tools beyond the device level for designing/analyzing such systems.



AMF microphotograph of silicon nanocrystals. The average nanocrystal radius is 3-4 nm. The average nanocrystal density is 10^{12} cm^{-2}.

This project aims to address these shortcomings though an integrated research effort at the nanoscale device, integrated CMOS circuit, and computer architecture levels. We are in the process of constructing a modeling environment whereby tradeoffs at each of these levels can be accurately and rapidly reflected in the other dimensions. One aspect of this work has involved the development of parametric models for electrical and optical components used in on-chip signaling, and the application of these models to guide the replacement of conventional electrical interconnects with optical components according to the specified design criteria. A result of this study is shown below. Here the power-delay product (PDP) is given for electrical and optical interconnect components for an interconnect length of 10mm. In 2008, the crossover point occurs where optical signaling becomes advantageous. By 2016, optical components achieve an order of magnitude advantage in PDP over electrical signaling. One of our current efforts involves devising microprocessor architectures that can best exploit the advantages of silicon nanoscale based on-chip optical signaling.



Power-delay product (PDP) comparison of electrical and optical interconnects for different technology nodes.

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