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NANO HIGHLIGHT
Metrology for Nanoelectronics

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Recently, Hutcheson[1] found that the device dimensions have become small enough to proclaim that chips are now nano-chips. The industry believes that extending CMOS technology through new materials and non-classical device structures will be possible for at least the next fifteen years. The gate length of these nanotransistors will shrink to less than 10 nm over this timeframe. As a result of reduced dimensions, the electrical properties of nano-transistors have moved into regime of short channel devices. Additional new physics will impact integrated circuit technology as scaling continues. Entirely new device structure are predicted for the nanoelectronics that will replace non-classical CMOS. This is referred to as Beyond CMOS. The astoundingly small size and high density of nanoelectronics will challenge metrology and characterization and most certainly move measurement further into the world of nanotechnology.

The long time goal of physical metrology is direct correlation of physical measurements with electrical properties. The new device physics of nanoelectronics is expected to impact measurement selection and application. On top of this challenge are the limitations and future needs of the measurement technology. Research and development require detailed materials characterization while the goal of metrology for is process control for each area of processing: Lithography, Front End Processes, and Interconnect.

The physics of nano-dimensions impacts more than just the device properties. For example, quantum confinement and surface states alter the optical properties of thin silicon layers in strained silicon on insulator (SOI) and other engineered substrates. Therefore, new optical models must be developed for measurement of thin film thickness and other properties. The gate dielectric on top of engineered substrates is one well-known example of thin, flat films. Strain engineering is being used to enhance mobility of the substrate below the gate dielectric. Strain also changes optical properties. Measurement of gate length will also be impacted by the new materials properties of thin lines and the engineered substrates below. For example, optical scatterometry is based on knowledge of the optical properties of the materials that form the patterned test structure. The optical properties of the bulk materials used to form sub 10 nm lines may be altered by the small line width. From what is known about nanoelectronics beyond CMOS, entirely new physics will dominate the properties of these materials and structures.

The introduction of new materials and the ultra-small dimensions of new devices have made materials characterization increasingly important. Transistor cross-sections are routinely imaged using transmission electron microscopy. The aberration of the lens in all but the newest TEMs introduce errors to film thickness determination using these images. Characterizing the electrical properties of interfaces between key device elements have become as critical as measuring the films themselves. The near-monolayer nature of these interfaces requires atom by atom characterization. The near atomic imaging ability of aberration corrected scanning electron microscopes is making them critical for scaling to the future.

References

1. G.D. Hutcheson, The First Nanochips, Scientific American, April, 2004, p48 – 55.