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Center for Nanoscale Systems in Information Technologies

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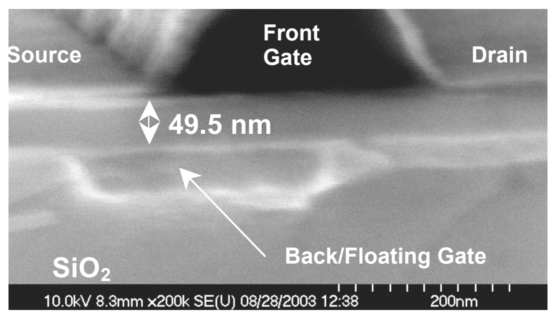
The Center for Nanoscale Systems (CNS) has assembled interdisciplinary teams to execute an aggressive and wide-ranging NSE research program with the goal of substantially advancing the impact of nanotechnology in future, high-performance, information technology systems [1]. CNS teams are working in three focused research thrusts – nanoelectronics, nanophotonics, and nanomagnetics – with the collective purpose of understanding and controlling the properties of materials at the nanoscale and of exploiting these material systems and associated nanoscale phenomena in technologically significant applications. The central objective is to develop effective nanoscale devices and systems that could be revolutionary solutions for the ever-more demanding requirements of future computational, sensing, storage and communication systems. CNS also seeks to develop and advance effective NSE research tools and techniques to support these information technology efforts. CNS is engaged as well in extensive and innovative NSE educational efforts at both the university and pre-collegiate level. Illustrative examples of current CNS research, educational and outreach efforts include the following:

Nanoelectronics: The CNS Si nanoelectronics thrust is focused on employing fundamental phenomena arising at the nanoscale in devices, technology, circuits, and architectures that address the challenges of achieving giant integration densities. These challenges range from accommodating the power dissipation in the shrinking area, obtaining reproducible operation with reduced statistics, the designability of circuits, and interfacing with the structures developed to take advantage of the nanoscale in the photonics and magnetics areas. Our approach is to develop new silicon-based technology and device structures and to incorporate them in simple circuits, and to demonstrate circuits and architectures that can be power adaptive and software programmable.



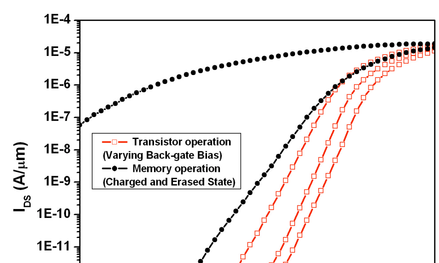


Fig. 1: Top: SEM x-section of back and front gated transistor structure. Bottom: Memory and transistor operation in a back-gated thin silicon geometry that is reducible to 10's of nm dimension.

This year we have shown that an innovative transistor structure, scaleable to 10 nm gate lengths, can be achieved with an exfoliation-based approach that allows us to produce thin (10's of nm) silicon layers with oxide and other electrode material structure on both sides. This enables a back-gated approach to transistors that can operate both as memory and as power-adaptive transistors. Fig. 1 shows the success of our approach: it demonstrates memory operation can be achieved by floating the back-gate and writing and erasing at high voltages, while good transistor operation is maintained at low voltages by applying bias to the back-gate. The uniqueness of the structure is in the achievable reduction in size and the decoupling of the storage from the sense operation.

The CNS carbon nanoelectronics goal is to create integrated electronic systems using molecules such as pentacene and carbon nanotubes as the active electronic elements. We further seek to integrate these new electronic materials into a standard Si environment to create hybrid Si/C systems. Major accomplishments over the past year are the reduction of nanotube and organic devices to nanometer-scale channel lengths. Bottom contact pentacene transistors were fabricated with channel lengths down to 30 nm using electron beam lithography and pentacene evaporation. The I-V characteristics of these organic transistors of record-breaking dimensions show saturation at just a few volts. We have also made important progress in the scaling of carbon nanotube transistors. Recently we have used an AFM tip as a moveable electrical contact to study the channel length scaling of nanotube devices down to 20 nm. On-state conductances within a factor of three of the ultimate limit of $4e^2/h$ predicted for a ballistic nanotube transistor have been observed.

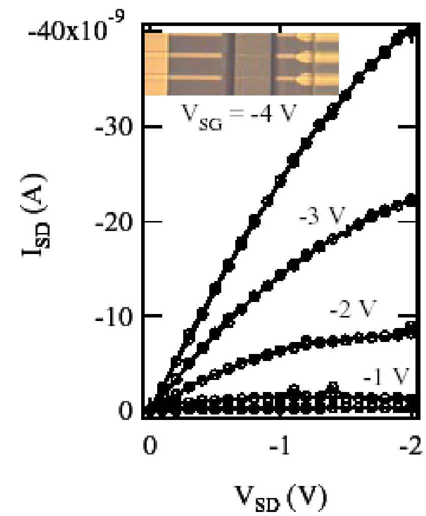


Fig. 2. I-V's at different gate voltages for pentacene transistors with 30 nm channel lengths. Upper inset: electrode pattern.

Nanophotonics: Photonic system components that exploit nanoscale phenomena to provide functionality could satisfy the full-spectrum of requirements for the future implementation of *all-optical* circuits and networks for telecommunications. The CNS approach is to manipulate the optical properties of materials by the utilization of nanostructures, e.g., quantum dots (QDs), and through nanoscale control and variation of composite materials.

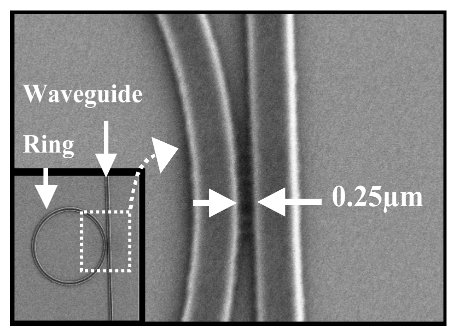


Fig. 3. Scanning electron micrograph that shows the top-view of a ring resonator coupled to a waveguide. Inset shows the entire ring structure. A pump pulse incident on the ring structure controls the transmission properties of a signal pulse sent through the waveguide.

A photonic circuit in which a light beam can control the flow of another beam is a longstanding goal for developing highly integrated optical communication components. It is highly desirable to use silicon - the dominant microelectronic material - as a platform for photonic chips. We have obtained the first experimental results of all-optical switching on silicon by using a highly confining structure to enhance the sensitivity of light to optically-induced refractive index changes and to minimize thermal effects. Under optical excitation, the structure can be made almost completely opaque or transparent, acting as an all-optical gate. The transmission of the structure can be modulated by more than 97% in less than 500 ps using light pulses with energies as low as 40 pJ.

Lead-salt QDs are among the few semiconductor materials to allow size-quantized optical transitions at technologically-important infrared wavelengths between 1 and 2 microns. One of the key questions in developing QDs for optical amplifiers is whether there exists a phonon "bottleneck" to intraband electron relaxation; rapid relaxation is highly desirable for amplifier applications. The presence of this bottleneck has been a controversial issue, and lead-salt QDs offer an ideal system for addressing this point because they have sparse energy spectra, with nearly complete symmetry between electron and hole single-particle states. We have performed a systematic study of intraband carrier relaxation in PbSe QD's, as a function of QD size and excited carrier density. Electrons are photo-created in 1p or higher states, and the population of the 1s state is monitored. We observe a rapid relaxation of the photo-excited electrons with the electrons relaxing over ~10 phonon energies in a few picoseconds. This result cannot be explained in the framework of any previously identified mechanism.

Nanomagnetics: The goal of the CNS nanomagnetics thrust is to advance the development of memory and signal-processing technologies that take advantage of the electron's spin as well as its charge. A major focus is on utilizing the potential to employ spin-polarized currents to control the dynamics of nanomagnetic moments in the 10-100 GHz regime, and on using torques from spin-polarized currents for possible applications in ultra-high density non-volatile on-chip memory applications. Within the last year, we have developed important new experimental techniques to measure, in both the frequency and real-time domains, the magnetic dynamics that result when a spin-polarized current applies a torque to an individual nanomagnet. We provided the first conclusive demonstration [3] that a DC spin-polarized current can generate microwave-frequency precession in a nanomagnet, and in fact by adjusting the applied current and magnetic field one can control the amplitude and frequency of the precession and also the nature of the motion among several distinct dynamical modes. We are investigating the application of these different modes for use in making field-tunable oscillators, microwave sources, and resonators. For memory applications, we are working to fabricate devices with reduced critical currents for spin-transfer-driven magnetic switching and also with higher resistances for better impedance-matching to silicon circuits.

NSE Education and Outreach: CNS in cooperation with Cornell academic units has undertaken substantial efforts to introduce students to nanotechnology, educate them in advanced NSE topics and thereby encourage them to pursue careers in NSE fields. One such effort has been the successful development of an introductory level course in NSE that includes a major hands-on laboratory component, which elucidates and compellingly demonstrates NSE concepts and techniques. This course was fully subscribed this fall and all of the students participating have indicated that they would and have strongly recommend the course. Nearly all have said that the course has motivated them to continue their study of NSE. In the area of educational outreach CNS offered two intensive summer courses for high school physics teachers in July 2003. More than 40 teachers participated in one or both courses, which spanned a total of three weeks. The courses emphasized NSE themes and included lectures by faculty and training on CNS take-home labs. At the conclusion, many teachers reported, "I feel re-energized about physics." Over 10 labs have been developed to date, and at least two-thirds of the teachers participating planned to use each one during the following school year. A fall one-day CNS workshop on the theme of "circuits" was attended by 28 teachers and 18 high school students. When asked how worthwhile the workshop was overall, teachers gave an average response of 4.8 (1= waste of time, 5 = extremely valuable). In the words of one teacher, "[I'll be] bringing back a lab plus a better sense of modern technology.... Students always ask about these things."

References

[1] For further information about this NSEC, link to **<www.cns.cornell.edu>** or email **<cns@cornell.edu>**
[2] "30 nm channel length pentacene transistors," Yuanjia Zhang, *et al.*, *Adv. Mater.*, **15**, 1632 (2003).

[3] S. Kiselev *et al. Nature,* **425,** 380 (2003)