# Nanotube and Nanowire Based Quantum Computation

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## Introduction

Our research efforts have been directed towards implementing a simple one-dimensional quantum computer using carbon nanotubes and silicon nanowires as the substrate, and at investigating issues of synthesis, nanofabrication, theoretical physics, and computer science surrounding this focused goal. The device on which we have concentrated consists of a one-dimensional string of islands of charge—quantum dots—with gate-controlled coupling between them. The spins of the dots are used to form the qubits of a quantum computer. It has been shown theoretically by one of the members of the team (DiVincenzo and coworkers) that a modulation of the coupling between neighboring elements in one dimension provides general computational power [1]; if the device ultimately operates as intended, it will function as a general purpose quantum computer.

The strength of the scheme lies in its simplicity. No dynamic g-factor modulation, no electron spin resonance, and no local magnetic fields are required to tune the qubits-only changes to the coupling between neighboring quantum dots along the nanotube or nanowire are necessary. This scheme has the further advantage that since operations only require nearest-neighbor coupling in 1D, scaling does not lead to a proliferation of interconnect elements.

## Research Overview

In the past year, the Marcus group has made two important steps toward multi-gated nanotube electronics. The first step was to develop a dielectric that allows top-gating of nanotubes without damaging the tubes. This investigation led to the development of an atomic layer deposition (ALD) liftoff method for high-dielectric-constant films [2]. It is worth noting that a positive lithographic process (such as liftoff) has not previously been achieved with ALD, and that such a process may be of wide interest in general semiconductor technology.

A first application of the conformal ALD insulting films to gated nanotubes is shown schematically in Fig. 1a, and in electron micrographs in Figs. 1b-d. To make these devices, Mo gates are deposited and subsequently covered with an ALD $HfO_2$ film. Then, tubes are grown by now-standard Fe-catalyst CVD methods. The resulting "undergate" structure (Fig. 1a) was not

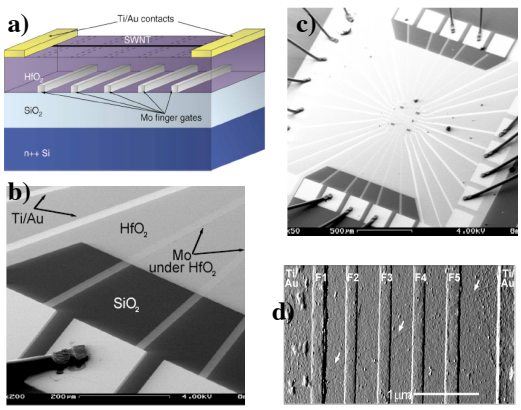


**Figure 1.** (a) Schematic of finger gating devices. Mo gates were defined using e-beam lithography on a Si/SiO2 substrate and subsequently coated with 25 nm of $HfO_2$ grown by low-temperature ALD. Nanotubes were grown across these local gates by CVD and contacted with Ti/Au electrodes. (b) Scanning electron micrograph showing complete device. (c) Higher magnification micrograph of ALD mesa edge (middle) showing Ti/Au wires on top of the mesa (upper left) and Mo wires running underneath the patterned ALD (bottom). (d). AFM image of nanotube grown across Mo finger gates and contacted (far left and far right) by Ti/Au leads. Arrows indicate the location of the nanotube.

successful in producing isolated gated dots, but was very useful for understanding how finger gates differ in their action from global back gates. These differences are shown in Fig. 2. What was learned from these measurements was that local gating predominantly affects the barriers between the nanotube and the metallic contact, rather than depleting the tube itself [3]. As a result, in order to produce local gating, it will be necessary to realize local "defect engineering" to make the tube depletable in a certain location. Local defect engineering is now underway using an AFM to make gateable defects in a tube using voltage pulses applied to the tube, and then aligning proximal electrostatic gates to those defects.

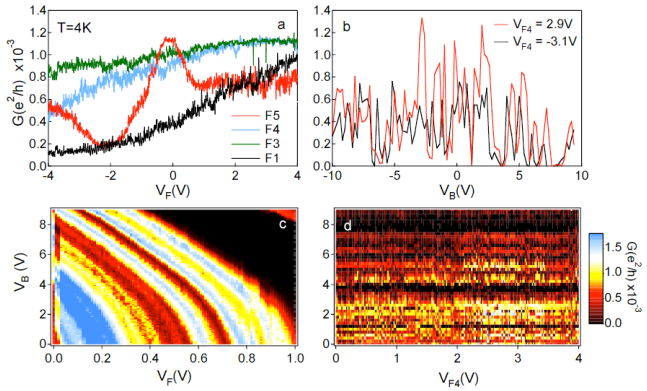


**Figure 2.** Transport measurements taken at 4K from the device in Fig. 1. (a) Conductance as a function of various finger gate voltages. (b) Line plot displays charging effects observed in sweeping the Si backgate. (c) 2D plot sweeping Si backgate voltage (VB) and finger gate voltage (VF) *while setting all fingergates to the same voltage*, indicating an additive effect between VB and VF. (d) 2D plot showing conductance as a function of $V_B$ and a single fingergate at $V_F$ with all others set to V=0. (See Ref. 3 for details.)

In addition to the nanotube studies by the Marcus group, the Lieber group has concentrated on the synthesis of molecular scale silicon nanowires [4,5]. The initial effort on growth and characterization has been focused on the preparation of intrinsic and p-doped Si nanowires with mean diameters of ~5 and 10 nm. Preliminary efforts in this area have recently shown that substantial improvements in the nanowire surface quality can be obtained through growth in hydrogen (Fig. 3). Key issues that must be addressed in this work, through careful studies of growth and TEM characterization, include control of nucleation to obtain narrow diameter distributions and control of overgrowth since finite size effects can change both nucleation and subsequent growth of small diameter nanowires.

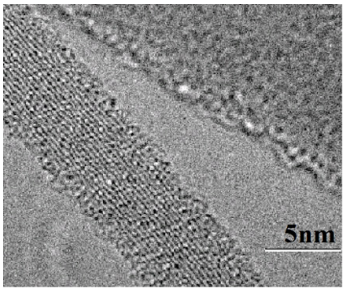


**Figure 3.** TEM image of single crystal 5.5 nm diameter silicon nanowire. The nanowires, which were grown in $H_2$ carrier gas, have <1 nm amorphous material at the surface.

In addition, significant effort has been placed on the fabrication and low-temperature transport studies of well-defined silicon nanowire devices. The emphasis of these studies has been on weakly coupled systems, which behave as single-electron devices, since these make it possible to investigate several issues of central importance to this project. Preliminary measurements on a 300 nm long 20 nm diameter Si nanowire device (Fig. 4) show clear coulomb blockade/single electron tunneling behavior. Significantly, analysis of these data yield a charging energy comparable to that calculated for this size nanowire device, thus suggesting that the mean free path is at least 300 nm long. The Lieber group is currently extending these intriguing

measurements to investigate the length dependence of the coulomb blockade/single electron charging phenomena for 20 nm devices at different fixed doping. An interesting issue will be to determine whether variations in the dopant distribution lead to localization on a length scale much smaller than the device since similar phenomena has been routinely observed in nanostructures fabricated from planar Si or SOI.

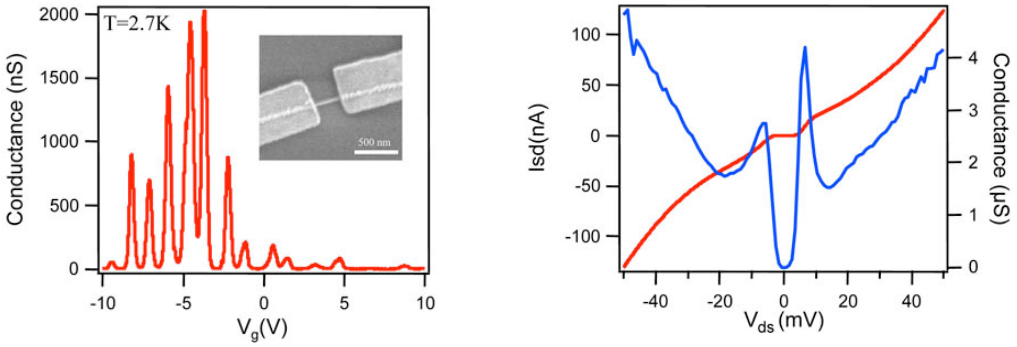


**Figure 4.** Coulomb blockade/single electron device data recorded on a ~300 nm long 20 nm diameter Si nanowire at 2.7 K. (left) Individual peaks in conductance vs. gate voltage correspond to changes in the sequential addition of single electrons to the device. (right) Current and calculated conductance vs. source-drain voltage at a minimum in the conductance vs. gate voltage. A clear gap—the coulomb charging energy—is observed.

Finally, our project has been advanced by theoretical insights of the Glazman group on transport of electrons in nanowires and quantum dots. The Glazman group has concentrated on electron-electron interaction effects in one-dimensional conductors [6], spin effects in quantum dots [7], and studies relating to the transfer of electrons along an array of quantum dots [8].

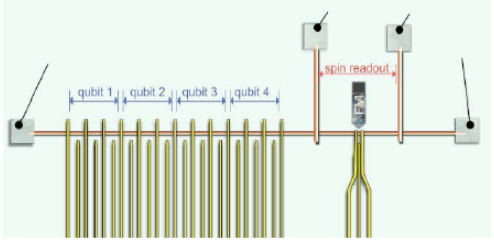


**Fig. 5.** Schematic of the complete device showing the essential elements of the proposal. The main ingredients are: a 1D array of quantum dots fabricated on a nanotube or nanowire, gate-controlled nearest-neighbor coupling, and a series spin detector to be used in a bucket-brigade readout.

**References**

[1] D. P. DiVincenzo, D. Bacon, J. Kempe, G. Burkard and K. B. Whaley, "Universal quantum computation with the exchange interaction", *Nature* **408**, 339-342 (2000).

[2] M. J. Biercuk, D. J. Monsma, C. M. Marcus, J. S. Becker and R. G. Gordon, "Low-temperature atomic-layer-deposition lift-off method for microelectronic and nanoelectronic applications", *Appl. Phys. Lett.* **83**, 2405-2407 (2003).

[3] M. J. Biercuk, N. Mason, and C. M. Marcus, "Local gating of carbon nanotubes", cond-mat/0308477.

[4] L.J. Lauhon, M.S. Gudiksen, D. Wang, and C.M. Lieber "Epitaxial Core-Shell and Core-Multi-Shell Nanowire Heterostructures," *Nature* **420**, 57-61 (2002).

[5] Y. Cui, Z. Zhong, D. Wang, W. Wang, and C.M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors" *Nano Letters* **3**, 149-152 (2003).

[6] Yu.V Nazarov and L.I. Glazman, "Resonant Tunneling of Interacting Electrons in a One-dimensional Wire", cond-mat/0209090.

[7] M. Pustilnik, L.I. Glazman, and W. Hofstetter, "Singlet-triplet Transition in a Lateral Quantum Dot", cond-mat/0304688; L.I. Glazman and M. Pustilnik, "Coulomb Blockade and Kondo Effect in Quantum Dots", cond-mat/0302159.

[8] A. Altland, L. I. Glazman, and A. Kamenev, "Electron Transport in Granular Metals", cond-mat/0305246.