NANO HIGHLIGHT
Single Crystal and Amorphous Nanoparticle Semiconductor Devices

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Researchers at the University of Minnesota have developed new techniques for producing, localizing, and integrating into transistor-like structures, single crystal cubes of silicon that are tens of nanometers on a side. Until this development, integrated circuits have been built using a single layer of transistors on the surface of a single crystal wafer. This only allows one to build circuits in two dimensions and does not generally allow one to mix different single crystal semiconductor materials on the same substrate. Alternatively, amorphous materials can be used in arbitrary combinations, but the performance is very poor compared to single crystal devices. This new development points toward the possibility of a variety of new technologies including 3D integrated circuits, integrated high-performance opto, magneto, and electronic devices on the same chip, and the formation of high performance devices on large area and low cost substrates.

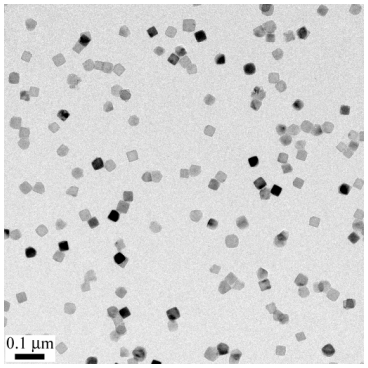

Fig 1 – Single crystal silicon cubes. The dark cubes are perfectly aligned with the microscope beam.

One of the primary discoveries of this group is a method for the production of single crystal silicon nanocubes[1,2]. The process uses an unstable silane plasma. The process creates an extremely high density plasma which, as shown at right, leads to a large concentration of small single crystal cubes with (100) faces. The crystallinity has been verified by high resolution electron microscopy.

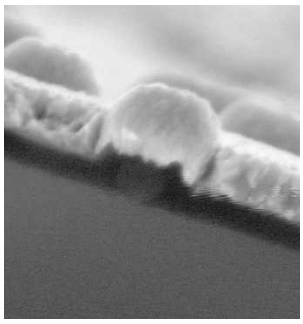

Fig 2 –Micrograph of contact to spherical amorphous nanoparticle.

In addition, researchers in this project have been working on localizing these particles using electrostatic self-assembly and on making electronic devices from the particles. We have succeeded in making metal-semiconductor-metal structures by depositing an insulator over the nanoparticles and using the topography to etch self-aligned holes in the insulator. Figure 2 shows a typical result for an amorphous nanoparticle device. We have been able measure the barrier heights of the contact structure and have gotten good metal-semiconductor-metal (MSM) performance. We are now working on vertical flow FET structures. In the area of self-assembly we have been able to localize metal particles to better than 100 nm, and are now working on localizing semiconductor particles.

References

[1] "Synthesis of Crystalline Silicon Nanoparticles in Low-Pressure Inductive Plasmas" A. Bapat, U. Kortshagen, S. A. Campbell, C. R. Perrey, C. B. Carter, Mat. Res. Soc. Proc. 2003.

[2] "Synthesis of highly oriented, single-crystal silicon nanoparticles in a low-pressure inductively coupled plasma" A. Bapat, C. R. Perrey, S. A. Campbell, C. B. Carter, and U. Kortshagen, J. Appl. Phys. **94**(3), 1969-1974 (2003).