PHONON TRANSPORT IN NANOSTRUCTURES WITH APPLICATION TO ULTRA-THIN SILICON-ON-INSULATOR (SOI) TRANSISTORS

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The fundamentals of phonon transport in nanostructures are not well understood at present. The continuum assumption fails in the *nanoscale* regime where either mean free path or wavelength of the phonons becomes comparable with the characteristic dimension of the nanostructures. Ballistic phonon transport in silicon films (*phonon-boundary scattering)* has been investigated through the large measured reductions in the lateral thermal conductivity compared to the bulk value [1], shown in Fig. 1. However, the phonon boundary scattering is not the only sub-continuum effect that occurs in nanoscales. The scaling of transistors has reduced the channel length and subsequently the size of the intense phonon-electron interactions in the active region of the transistor. The small size of the phonon source compared to the phonon mean free path may yield dramatically larger transistor temperatures than those predicted using the Fourier law of heat diffusion (Fig. 2). This results from the ballistic, or non-local, nature of phonon conduction near a small heat source.

Thermal design of microelectronic devices demands accurate characterization of the thermal transport properties of the thin films and nanostructures. In particular, the effect of ballistic transport near a small heat source, which has greater implications for transistors, has not been experimentally investigated. High spatial and temporal resolution diagnostic tools (at room and cryogenic temperatures) are needed to map the rapid and localized heating during an electrostatic discharge event. Simultaneous treatment of charge and phonon transport with characteristic length scales spanning several orders of magnitude is required to provide design guidelines for future generation of submicron transistors. At present, simulation and understanding of sub-continuum phonon transport in bulk and SOI transistors *lag* behind the state-of-the-art charge transport simulation tools available to the semiconductor industry.

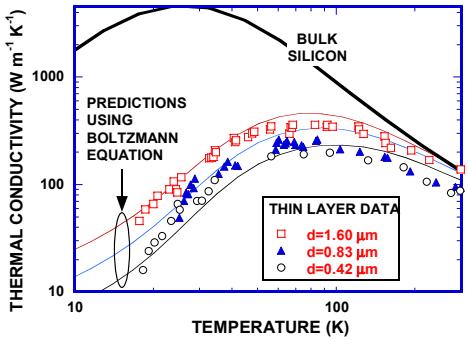

Fig. 1. Thermal conductivity of single-crystal silicon layers with different thicknesses is compared with bulk values [1]. Predictions are based on the Boltzmann transport equation (BTE).

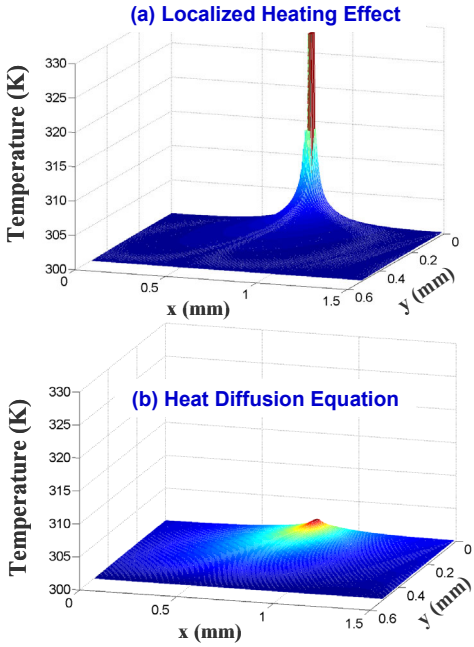

Fig. 2. Temperature profile in the 0.12 μm NMOS. For this particular case, the dimension of the hot spot is about r = 12 nm. The predicted maximum temperature rise using the BTE and heat diffusion equation are 328 K and 302 K, respectively, which reveals that using conventional heat diffusion equation significantly underestimates the peak temperature of the transistor.

This project is focusing on the study of two major nanoscale phenomena: (a) phonon transport in single crystal silicon layers of thickness in the range of 10-50 nm and, (b) ballistic phonon transport near hotspots (~10 nm) in the active region of silicon-on-insulator (SOI) transistors. The experimental part of our effort involves the very first measurements of thermal conductivity of nanometer size, single crystal silicon nanostructures as well as the ballistic phonon transport near a hotspot in a transistor. Several nanostructures have been designed to measure the thermal conductivities of the electrically conductive [2] (*e.g.*, doped silicon and metallic multilayers) and dielectric layers (*e.g.*, silicon). The thin film structures are deposited on the top of a thick silicon dioxide layers, which acts as a thermal barrier that forces heat to spread along the overlayer before it reaches the substrate. The Joule-heating and thermometry along the patterned nanostructure results in a temperature distribution that strongly depends on the film lateral thermal conductivity. This technique allows simultaneous electrical and thermal conductivity measurements of the ultra thin (10-50 nm) and narrow (widths, 10-20 nm) electrically conductive layers, which are impossible to fabricate in the form of suspended structures. In addition, we have also succeeded to fabricate and to perform thermal conductivity measurements on suspended giant magnetoresistive (GMR) beams of thickness ~100 nm [2]. A careful sensitivity analysis has shown that these beams will enable us to measure the thermal transport properties of silicon layers of thickness near 10 nm.

The transient and steady state heat transfer experiments on nanostructures, at both room and cryogenic temperatures, will be performed to reveal the fundamentals of phonon transport in the nanoscales. A state-of-the-art thermal reflectance setup is currently constructed that enables thermometry of submicron structures with spatial resolution near 400 nm and temporal resolution near 5 ns in the temperature range of 4-450 K.

Three numerical approaches are undertaken for predicting nanoscale thermal phenomena in semiconductors: (a) Molecular Dynamic techniques, which simulate the lattice vibrations [3]. Here the transport coefficients (*e.g.,* heat conductivity) can be obtained, in principle, from the atoms' position, velocity, and interatomic potential by the modified Green-Kubo formula using time-dependent correlation functions. This approach does not require modeling of phonon interaction with other phonons, boundaries, material interfaces, vacancies, or impurities. (b) Boltzmann Transport Equation (BTE) solution, which simulates phonon transport in the relaxation time approximation, using a structured finite volume method and considering the heat generation in the silicon device layer of a sub-micron transistor [4]. Significant simplifications are made because, either the actual phenomena is not well understood (scattering processes among different phonon polarizations, phonon branches, and scattering with material interfaces) or its numerical implementation is complex (location, direction, and frequency dependent relaxation times).

The analytical work will take advantage of the experimental data and numerical simulations to introduce *simple*, yet *physically realistic*, expressions for phonon transport in nanostructures, which can be used for rapid electrical/thermal simulation. Fig. 3 shows the steady state predictions for maximum temperature rise in the next generation submicron transistors, using both the heat diffusion equation and an approximate solution of the BTE. The results indicate that the local temperature rise in the hot spot region increases, even though device power dissipation decreases, with the minimum device feature size. At the doping levels of current technology ($> 10^{18}$ cm^{-3}), the temperature rise required for a thermal runaway failure exceeds 1000°C [5]. This implies that the failure will not occur during normal operation of the transistor. The effect of local hot spot may be observable through a reduction in the electrical carrier

mobility; however, the use of fitting parameters in electrical mobility modeling may mask this effect [5]. If the doping is reduced to the concentrations near 10^{17} cm^{-3} the critical temperature will be near 700 K, then the localized heating should be taken into account. The effect of localized heating during the transient operation of the device and ESD event will be more significant and is currently under investigation.

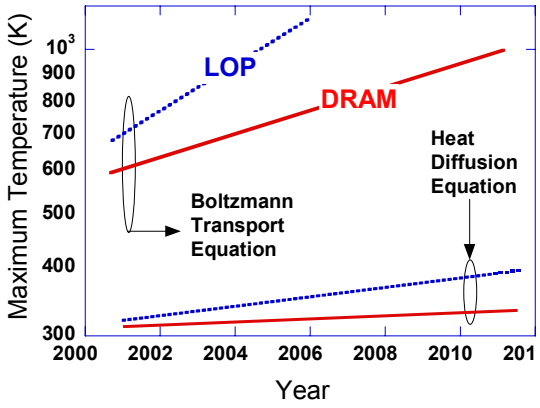

Fig. 3. The steady state predictions for maximum temperature rise in the future generation submicron transistors using both the heat diffusion equation and an approximate solution of the BTE.

The multidisciplinary faculty from the Mechanical, Electrical and Computer, and Chemical Engineering departments who have undertaken this project combine strengths in solid-state physics, heat transfer, fabrication processes and advanced experimental/numerical techniques. IBM, the industry leader in the design and fabrication of SOI transistors, strongly supports our research activities and will collaborate with us in the following areas: (a) fabrication of the structures for thermal conductivity measurements; (b) integration of simulation tools for charge and phonon transport in transistors; and (c) measurements of the self-heating effect and ESD phenomenon in the SOI devices.

The impact of the present study will not be limited to the semiconductor industry. It appears that many of the emerging technologies in data storage rely heavily on energy transport at the extremely short time and length scales as a mean to overcome the superparamagnetic limit - a serious impediment to future advancement of the storage technology [6]. Additionally, thermally induced failure and reliability issues at the nanoscale levels are becoming increasingly important due to rapid device miniaturization in the data storage applications. Further advances in high-technology data storage systems will be difficult, if not impossible, without rigorous treatment of the nanoscale energy transport.

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