Semiconductor Nanowires: Building Blocks for Nanoscale Electronics

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Project Objectives

Semiconductor nanowires are attracting increasing interest due to their potential to serve as basic building blocks in a bottom-up fabrication scheme for nanoscale devices and circuits. In order to realize this goal, it is necessary to control the nanowire composition, size, conductivity and other physical properties; assemble the wires into rational device geometries; and enable current flow between nanoscale and microscale structures. Furthermore, it is essential to understand the impact of restricted size and surface effects on the electrical properties of these structures. In this program, we are developing a versatile, template-based approach to the synthesis of metal/semiconductor/metal nanowires. This method utilizes nanoporous membranes as substrates for nanowire assembly using semiconductor vapor-liquid-solid growth and metal electrodeposition. After removing the wires from the membrane, a field assisted assembly method is used to attract and align the nanowires on to pre-patterned contact pads on a substrate. This technique utilizes a nonuniform electric field to polarize the nanowires and induce alignment via dielectrophoresis. The structures and techniques developed in this program are used to carry out detailed experimental studies of electrical transport in semiconductor nanowires and metal-semiconductor nanocontacts. Theoretical models of band structure and carrier scattering are also being developed to provide insight into the fundamental transport mechanisms in the wires.

Nanowire Synthesis

The nanowire synthesis technique developed in this program, shown schematically in Figure 1, combines two different approaches which are currently used for nanowire fabrication; template-directed synthesis utilizing nanoporous materials and metal catalyzed vapor-liquid-solid growth. In the first approach, nanoporous materials are used as templates for nanowire synthesis via pore filling methods such as electrodeposition or chemical vapor deposition. The nanowire diameter is determined by the pore size, which can range from approximately 10 nanometers to greater than 200 nanometers. The direct deposition of silicon into a nanopore using chemical vapor deposition, however, yields polycrystalline material. Alternatively, vapor-liquid-solid growth has been used to produce single crystal semiconductor nanowires such as silicon and gallium arsenide. In this approach, gold is used to form a liquid eutectic alloy with silicon at 363ºC, which, upon supersaturation, nucleates the growth of a silicon wire. The nanowire diameter, in this case, is determined by the size of the initial gold particle. In combining the two techniques, we have been able to grow silicon nanowires up to 30 microns in length with controlled diameters

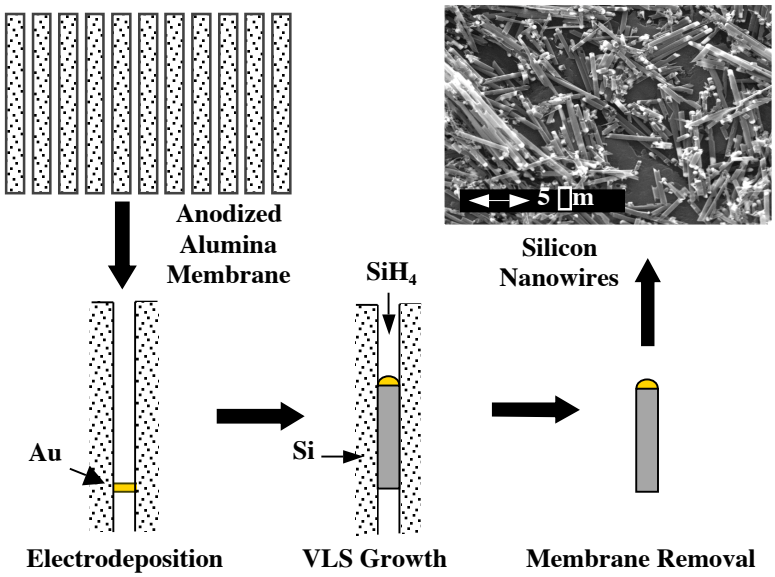

Figure 1. Schematic of nanowire fabrication process.

ranging from 80 nanometers to over 200 nanometers [1,2]. TEM characterization revealed that the nanowires are either single crystal or bicrystal with a (111) twin boundary running along the axis of the wire [3]. Boron-doped silicon nanowires were fabricated using trimethylboron as the dopant source.

Nanocontact Formation

We have succeeded in fabricating multilayered metal/semiconductor/metal nanowires by electrodepositing metals such as cobalt, rhodium and platinum into the membrane pores prior to electrodepositing gold and performing vapor-liquid-solid growth of silicon. A transmission electron microscopy image of a Au/Si/Rh nanowire produced by this technique is shown in Figure 2. By using the correct amount of gold in the pore, all of the gold travels along the tip of the growing silicon nanowire. The other metal (such as cobalt) comes into contact with silicon and reacts to form a metal silicide, resulting in a multilayer such as cobalt silicide/silicon/gold [4]. The alumina membranes are then etched away to release the nanowires for structural and electrical characterization. The versatility of this fabrication technique offers the potential to select different metal/semiconductor combinations, different wire diameters, and different doping densities to facilitate the study of size effects in metal/semiconductor contacts. The technique will also allow us to link together semiconductor nanowires of different conductivity and type to produce unique structures with increased functionality and reduced size.

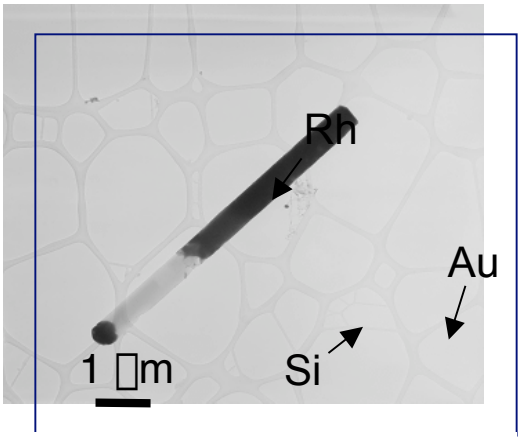

Figure 2. TEM image of Au/Si/Rh nanowire. Silicide growth is anticipated between the Si and Rh.

Nanowire Assembly and Electrical Characterization

The electrical properties of the nanowires synthesized in this program are being characterized using variable temperature 4-point resistivity and gate-dependent source-to-drain current measurements. After the nanowires are grown and removed from the template, they are aligned between pairs of predefined electrodes on an insulating substrate to facilitate electrical characterization. This assembly technique, which relies on forces induced on the nanowires due to their polarization in a nonuniform electric field, has been used to align with high yield silicon nanowires with diameter ranging from 80 – 250 nm and length 4 – 15 □m. Following alignment, electron beam lithography is used to pattern two additional metal contacts, which serve as the voltage probe during the 4-point measurement. An SEM image of a 100-nm diameter silicon nanowire prepared using this fabrication approach is shown in Fig. 3. We are currently measuring the 2- and 4-point resistivity of undoped and boron-doped silicon nanowires as a function of temperature to study the effect of nanowire diameter and doping on their electrical transport properties. We have also prepared samples that contain a back metal gate

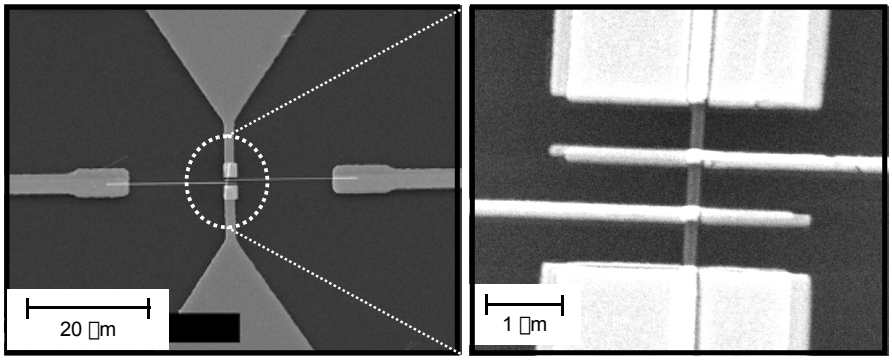

Figure 3. SEM image of 4-point silicon nanowire resistivity measurement structure. Left: Low magnification image of the four contacts to the nanowire: two for forcing current and two for measuring voltage. Right: High magnification image of 100-nm diameter silicon nanowire contacted at its tips by large area pads and in the center with metal contacts defined by electron beam lithography.

for measuring the dependence of the source-to-drain current on the applied gate voltage to determine the doping type (n- or p-) of the undoped and intentionally doped nanowires. These back-gated samples will also be used to evaluate the field effect properties of the silicon nanowire devices for use in electronic circuit applications, which include high-density logic and heterogeneously integrated sensors. We are employing similar techniques to study large-area ohmic contact formation to the nanowire tips, and to isolate electrically silicide-silicon nanocontact junctions.

Theory

A powerful and flexible method for the numerical solution of the semi-classical Boltzmann transport equation in a cylindrical geometry has been conceived and tested. A principal objective of this initial computational work is to understand and to study finite-size effects and the conductance of large (≥100 nm diameter) semiconductor nanowires. We have focused some attention on the magnetoresistive effect, the existing semi-classical theories of which involve restrictive assumptions, and further, may be inadequate to explain very recent experimental findings.

The numerical studies were carried out in a Maxwellian regime with an isotropic and parabolic electron dispersion relation. Calculations were made in the relaxation-time approximation, with radial variation of the relaxation time to include the effect of the surface. We computed the reduction in conductivity due to enhanced surface scattering, for wires of various radii and relaxation times, as shown in Figure 4. Surface effects become most pronounced when electrons explore the wire throughly as a result of long relaxation times or a high temperature. A magnetic field can keep electrons from straying to the surface and scattering; it does this most effectively when the electrons have long scattering times that lead to long periods of confining magnetic force between scattering events. Currently, the numerical scheme is being adapted to study the specific case of silicon nanowires.

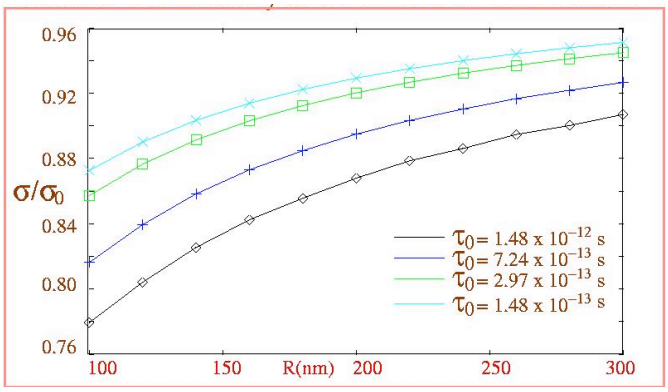

Figure 4. Relative conductivity, □/□o, as a function of nanowire radius, R, at 300K. □o is the bulk conductivity corresponding to scattering time □b.

Future

Our initial results have laid the groundwork for further studies of finite-size effects on electrical transport in semiconductor nanowires and nanocontacts. Work is currently underway to investigate the impact of wire diameter, doping level, surface treatment and contact metal on carrier transport as well as to extend these studies to III-V semiconductors. This information is vital to the design and operation of future devices that employ these nanostructures such as field-effect transisitors, chemical and biological sensors and nanoscale optical devices.

References

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