*NIRT Highlight (Devices and Architectures)*

# PHONON TRANSPORT IN NANOSTRUCTURES WITH APPLICATION TO ULTRA-THIN SILICON-ON-INSULATOR (SOI) TRANSISTORS

The fundamentals of heat carrier (e.g., phonon and electron) transport in nanostructures are not well understood at present. The continuum assumption fails in the *nanoscale* regime, where either the mean free path or the wavelength of the phonons becomes comparable with the characteristic dimension of nanostructures. This project will focus on the study of two major nanoscale phenomena: (a) phonon transport in single crystal silicon layers of thickness in the range of 10-50 nm and (b) ballistic phonon transport near hotspots (~10 nm) in the active region of silicon-on-insulator (SOI) transistors (Figure 1).

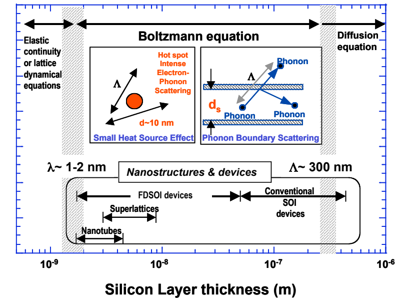


**Figure 1: Regime map for phonon transport in ultra-thin silicon layers.**

The experimental part of our effort involves the very first measurements of thermal conductivity of nanometer size, single crystal silicon nanostructures as well as the ballistic phonon transport near a hotspot in a transistor. Several nanostructures have been designed to accomplish these tasks. The design of these structures requires careful and rigorous nanoscale heat conduction and sensitivity analysis. In addition, the temperature measurements at room and cryogenic temperatures demand the implementation of high (temporal and spatial) resolution thermometry techniques (Asheghi and Yang, 2002). As part of this project, the PI is established an integrated high-resolution electrical and optical probing facility for thermometry of nano (micro) -devices and structures.

The measurement structures shown in Figure 2 will be used to measure the thermal conductivities of the electrically conductive layers (e.g., doped silicon and metallic superlattice). The thick silicon dioxide layer acts as a thermal barrier that forces heat to spread along the overlayer before it reaches the substrate. The Joule-heating and thermometry along the length of the patterned nanostructure results in a temperature distribution that is strongly dependent on the lateral conduction along the film. This technique allows simultaneous measurements of electrical and thermal conductivities of ultra thin (10-50nm) and narrow width (10-20 nm) electrically conductive layers, which are impossible to fabricate in the form of suspended structures (Yang et al., 2002).

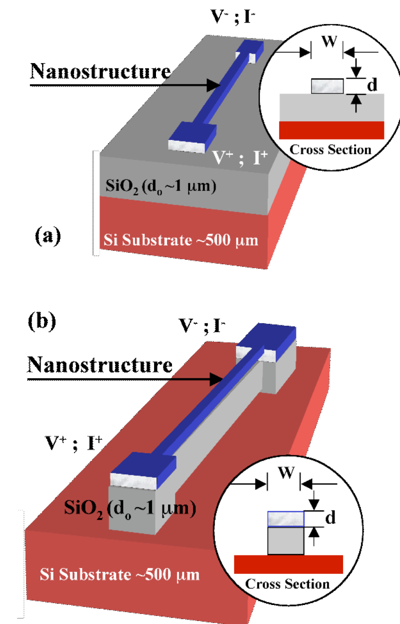


**Figure 2: Cross section of the experimental structures.**

Figure 3 shows the relative electrical resistance change that can be achieved for 10% variation in the thermal conductivity of the electrically conductive nanostructure, for different experimental measurement techniques. The sensitivity of the structures shown in figure 2 are compared to the suspended beam structure which has the highest sensitivity among all these approaches; however, it involves more elaborate fabrication process that may not be feasible for extremely narrow width and thin nanostructures.

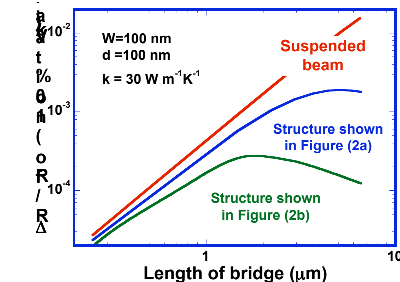


**Figure 3: Relative electrical resistance change in the metal bridge for 10% variation in thermal conductivity of the nanostructures.**

*References:*

Mehdi Asheghi; Cristina H. Amon, Gary K. Fedder , Myung S. Jhon, and Shi-Chune Yao ; NSF award 0103082, Carnegie Mellon University.

Asheghi, M., and Yang, Y., 2002, "Micro- and Nano- Scale Diagnostic Techniques for Thermometry and Thermal Imaging of Microelectronic and Data Storage Devices," in *Micro- and Nano-Scale Diagnostic Techniques*, Kenny Breuer, ed., Springer-verlag. In press.

Yang Y., Liu W., Shojaeizadeh S., Zhang, S. and **Asheghi M.**, 2002, "Thermal Property Measurements of Giant Magnetoresistive (GMR) Layers," to be presented at the ASME International Mechanical Engineering Congress & Exposition, Paper No. HT-32782, November 17-22, 2002, New Orleans, Louisiana.