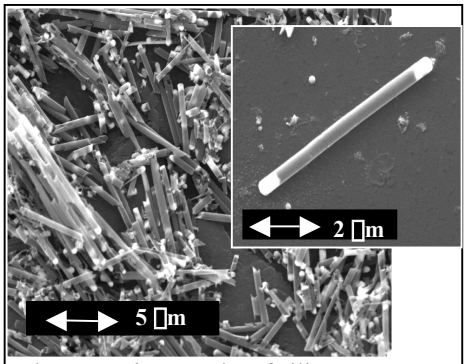
NIRT Highlight

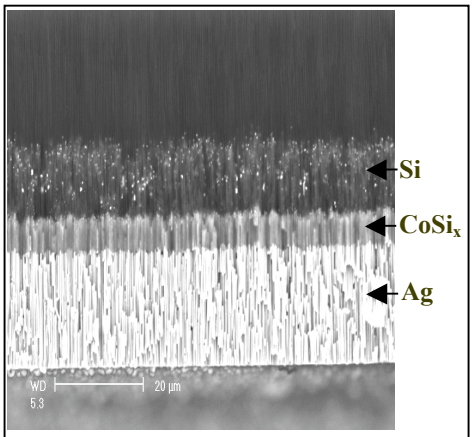
Semiconductor Nanowires: Building Blocks for Nanoscale Devices

Researchers at Penn State University have developed a new method for the synthesis of single crystal silicon nanowires that provides good control over the diameter and aspect ratio of these structures and also enables the fabrication of multilayered metal-semiconductor nanowires. The Penn State team, which includes faculty members from materials science and engineering (Joan Redwing and Suzanne Mohney), electrical engineering (Theresa Mayer) and physics (Ari Mizel) plan to use the nanowires to study electrical transport and metal/semiconductor contact characteristics in small dimensional structures. Semiconductor nanowires may ultimately serve as building blocks in future nanoscale device architectures with applications in chemical and biological sensing, nanoelectronics and photonics.

The technique developed at Penn State combines two different approaches which are currently used for nanowire fabrication; template-directed synthesis utilizing nanoporous materials and metal catalyzed vapor-liquid-solid growth. In the first approach, nanoporous materials are used as templates for nanowire synthesis via pore filling methods such as electrodeposition or chemical vapor deposition. The nanowire diameter is determined by the pore size which can range from 5 nanometers to greater than 200 nanometers. The direct deposition of silicon into a nanopore using chemical vapor deposition, however, yields polycrystalline material. Alternatively, vapor-liquid-solid growth has been used to produce single crystal semiconductor nanowires such as silicon and gallium arsenide. In this approach, gold is used to form a liquid eutectic alloy with silicon at 363^{o}C, which, upon supersaturation, nucleates the growth of a silicon wire. The nanowire diameter, in this case, is determined by the size of the initial gold particle. In combining the two techniques, the researchers at Penn State have been able to grow single crystal silicon nanowires up to 30 microns in length with diameters ranging from 130 nanometers to 200 nanometers within the pores of anodized aluminum membranes. Furthermore, by electrodepositing metals such as cobalt and platinum into the pores prior to silicon growth, the researchers have succeeded in fabricating multilayered metal/semiconductor nanowires such as gold-silicon-cobalt silicide and gold-silicon-platinum. The alumina membranes were etched away following growth to release the nanowires for structural and electrical characterization. The versatility of this fabrication technique offers the potential to select optimum metal/semiconductor combinations and link together semiconductor nanowires of different conductivity and type to produce unique structures with increased functionality and reduced size.



Electron micrographs of silicon nanowires produced by template-directed vapor-liquid-solid growth after release from membrane.



Electron micrograph of cross-section of silicon-cobalt silicide nanowires prior to removal from membrane. The silver layer is used to provide backside contact for the electrodeposition process.

Relevant References:

"Bicrystalline Silicon Nanowires", A.H. Carim, K.K. Lew and J.M. Redwing, Advanced Materials **13**, 1489 (2001).
"Template-directed vapor-liquid-solid growth of silicon nanowires," K.K. Lew, C. Reuther, A.H. Carim, J.M. Redwing and B. R. Martin, Journal of Vacuum Science and Technology B **20**, 389 (2002).

(DMR-0103068)

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