Semiconductor Industry Research Needs in the Nanotechnologies

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1. Introduction

For over a decade, the semiconductor industry has published a consensus document, now called the International Technology Roadmap for Semiconductors (ITRS) that identifies anticipated technology needs. ITRS's primary goal is to continue the exponential increases in functionality per unit cost, as characterized by Moore's law. Each version of the ITRC technology cadence has featured acceleration of the pace of scaling; albeit while placing increased demands on the technologies required to realize the accelerated pace. The net effect of ITRS acceleration has been that the horizon for unsolved problems has moved closer to the present, to the point that there are now technology areas for which no known solutions exist that are within the five-year horizon. Many of these challenges will require the introduction of new materials and processes at an unprecedented pace and substantial changes in device architectures will be needed.

Leading edge production in the industry is approaching the 100 nm technology node and within ten to fifteen years, we expect feature sizes in production to be approaching 10 nm. In order to continue the pace of semiconductor technology forecast by the ITRS, it will be essential that new physical understanding be developed for nanoscale processes, materials, interfaces, design methods, and system architectures. We believe that the National Nanotechnology Initiative can be an important resource for the industry as it faces these challenges.

2. Ultimate CMOS

The end of CMOS scaling is foreseeable, although the specific combination of factors that will end scaling is not known. As industry moves through the two to three year technology generation cycles, the complexity of the processes is increasing and the demands on fabrication equipment performance are more strenuous. For example, in order to construct 25 nm devices, lithography tools are needed that operate beyond optical lithography limits. Fortunately, there are several technology options; however an extremely costly R&D effort is required to translate these technologies into production tools in about one decade. The performance of the scaled device in the 25 nm regime is itself problematical. The gate oxide has been aggressively scaled to enhance device performance. However, as the thickness of the gate approaches 1 nm through scaling, tunneling through the gate oxide creates unacceptably large off currents, dramatically increasing quiescent power consumption, and rendering the device impractical for analog applications due to unacceptable noise levels.

We project that the evolution of the bulk planar CMOS device will plateau around the 25 nm technology node and that these devices will find their primary use in products for which performance is a tantamount consideration, and power consumption is not a primary driver. Analog applications of bulk CMOS technology likely will lag about two technology nodes behind high performance digital and may coexist on the same chip. Analog design may be facilitated by incorporation of SiGe bipolar devices on the same chip. At the limit, bulk CMOS devices may not suffice for low power applications.

There are several technology options that may extend CMOS technology beyond 25 nm. Various forms of dual gate devices have been proposed as possible options for CMOS. The use of dual gates can be shown to increase current drive for the transistor. However, the processes required to fabricate dual gate devices are very complex, demanding, for example, precise alignment of the gates. Other options that show a promise to extend CMOS technology include silicon-on-insulator technologies and cooled CMOS devices. It has been projected that by exercising some or all of these options, CMOS technologies might be extended to the 10 nm technology node [1].

Density scaling will gradually give way to functional scaling where the focus will be on the effective utilization of transistors and interconnects. This will probably add new functions to CMOS that will lead to hybrid technology integration at the die, package and board levels. New 3D structures will be needed at the nano, meso and macro levels to move information and heat.

As we see it, the physical and chemical understanding necessary to reach the ultimate limits of CMOS technology also will provide the basis for inventing new technologies that will eventually supplement CMOS.

3. Research Needs in Semiconductor Basic Sciences

SRC, on behalf of the semiconductor industry, has developed a list of nanoscale topics requiring substantial research if the ITRS cadence is to be sustained. These are given in abbreviated form below.

A. Nanoscale Physics and Chemistry

- **The Physics of Interfaces**
  - ⇒ interface architectures for nanoelectronic devices
  - ⇒ transport properties in interface dominated nanosystems
  - ⇒ Correlate atomic structures with interface mechanical properties
  - ⇒ environmental factors and local functional groups (e.g. surface adsorbates)
  - ⇒ effects on electronic properties of nanostructures
  - ⇒ geometry-dependent properties of nanostructures
  - ⇒ number of atoms and specified properties of interfaces

- **Conductivity at small dimensions**
  - ⇒ conductivity in mesoscopic, molecular, and atomic wires
  - ⇒ atomic wires on different substrate materials
  - ⇒ electron transport in single molecules
  - ⇒ conductivity quantization in nano MOSFET channels
  - ⇒ metal-dielectric interconnects: manufacturing & reliability

- **Deterministic doping effects**
  - ⇒ structure-property relations for design: band gap, dielectric constant, mobility, etc
  - ⇒ manipulation of single dopant atoms
  - ⇒ nanoscale arrays of dopants
  - ⇒ metrology techniques for single dopant positions, types, and states
  - ⇒ stability of doped structures

- **Functional Synergy in Electronic Materials**
  - ⇒ Measure spin phenomena at the single-spin level
  - ⇒ Optical spin-injection devices's without electrical connections
  - ⇒ biomimetic and biocompatible systems
  - ⇒ intelligent and evolving materials
  - ⇒ molecular electronics & Nano-Electromechanical Systems (NEMS)
  - ⇒ doping, nanoporous electronic materials, defect engineering
  - ⇒ "architectonic" Quantum Dots Solids
  - ⇒ collective behavior (i.e. synergetics) effects in solids
  - ⇒ entanglement and quantum decoherence
  - ⇒ qubits based on solid-state concepts mobile qbits and transport of entangled qbits
  - ⇒ large-scale controlled entanglements
  - ⇒ picosecond optical excitation quantum-dot states
  - ⇒ basic materials data

B. Nanoscale Materials

- **Nanoparticles and Nanotubes**
  - ⇒ physical properties
  - ⇒ control size, distribution, molecular architecture
  - ⇒ electronic properties as function of size and structure
  - ⇒ "Fine tune" the electrical, optical, mechanical, and sensing properties by compositional and size control
  - ⇒ Extend the nomenclature of calibrated nanomaterials
  - ⇒ assemblies of different types of nanotubes into networks and functional systems

- **Metrology of Nanoscale Materials**
  - ⇒ noninvasive tools to determine correlations between structure, macroscopic properties, functionality
  - ⇒ local environment & functionality of embedded components
  - ⇒ enhanced interface spectroscopies
  - ⇒ tools for functionality in complex assemblies

⇒ models for energy transfer and dissipation mechanisms

C. Nanoscale Devices

- **Molecular Devices**
  - ⇒ functionality by combining individual molecular devices
  - ⇒ electron transport through a molecule
  - ⇒ materials nomenclature for molecular design
  - ⇒ three-terminal molecular and nanoscale devices with gain
  - ⇒ molecular and orbital level electrical contacts
  - ⇒ nanoscale cross-wire and wireless interconnect architectures

- **Single electron devices**
  - ⇒ single electron transistor (SET) memory
  - ⇒ fabrication methods for mass production
  - ⇒ limitations of single electron logic
  - ⇒ phase-shift and tunneling phase logic
  - ⇒ optimum materials for single electron devices, circuits, and systems

- **Deterministic-doping devices**

  - ⇒ manipulation of atoms/ molecule interactions with surfaces materials

D. Molecular and Nanoscale Fabrication Methods and Processes

- **Self-assembly:Near-term**
  - ⇒ hybrid approaches, such as photolithography modulated self assembly
  - ⇒ self assembled resists for advanced lithographies
  - ⇒ database of structure-property relationships, synthetic methods
  - ⇒ Bulk properties and processes catalogued
  - ⇒ dendrimers and composite dendrimer systems

- **Self-assembly:Medium-term**
  - ⇒ electronic/optical applications, retinal cone-like structures for optical image processing.
  - ⇒ Molecular printing and alignment
  - ⇒ Self assembled MEMS
  - ⇒ Self assembled optical interconnects
  - ⇒ Polymer-based electronic devices, circuits, and systems
  - ⇒ Bio-inspired manufacturing, assisted self assembly

- **Nano-metrology, -lithographic Patterning**
  - ⇒ unimolecular pixels
  - ⇒ chemically inhomogeneous materials- block copolymers
  - ⇒ certified nanotip and nanotube probes
  - ⇒ atomic manipulation of dopants
  - ⇒ strategies for massive amounts of information
  - ⇒ coupling between molecules & their surroundings
  - ⇒ physical/chemical linkers & junction electronic properties
  - ⇒ patterning nonregular structures on substrates
  - ⇒ electrical contacts to outside world & internal interfaces